MOTOROLA

Chip Errata

68307 Integrated Multiple-Bus Processor

August 21, 1995 (Parts Not Suitable for New Designs)

Contents of this document are intended only for the internal use of Motorola customers designing with this product.

The mask set for each part is encoded into the device topside markings - for example, the following markings would indicate a device from the 0F37C mask, manufactured in the 18th week of 1994:

XC68307FG16
0F37C
IEAD9418

This errata list applies to the following 68307 mask sets:

Rev.	Mask	Processing Geometry	Part Number Suffix
A	0F37C	0.8u	(none)
B	1F37C	0.8u	(none)
C	G57B	0.8u	(none)

1. UART Never-Ending Break

If a Start Break command is written to a UART Command Register, followed by a Stop Break command to the same register, followed by some other command to the same register, then the transmit data will go low (start break) then high (stop break) then low again (a new break is issued erroneously when the last command is written and will not go away.)

Workaround:

Whenever a Start Break or Stop Break command is issued, follow immediately with a No Command command (00). Other commands can be issued any time, even between a Start Break/No Command or Stop Break/No Command pair.

Masks: 0F37 1F37 G57B Date: 3/11/94

2. UART Receive Buffer Data Corrupt

If the UART receiver is set to operate in five bits-per-character mode and the receiver FIFO is full, data read from the receiver may be corrupt. This condition may be exaggerated at low temperatures and extreme V_{cc}.

Workaround:

Use more bits per character or don't allow the receiver FIFO to become full.

Masks: 0F37 1F37 G57B Date: 3/11/94

3. UART Timer Period

The timer period of the 68681 is 2 x (timer_load_value) x timer_clock_period. The timer period of the 68307 UART is 2 x (timer_load_value + 1) x timer_clock_period.

Workaround:

Compensate the timer_load_value. The 68307 UART timer is capable of generating all frequencies that the standalone 68681 timer can generate. The minimum timer_load_value of the 68681 is two; the minimum timer_load_value of the 68307 UART is one, which creates the same frequency.

Masks: 0F37 1F37 G57B Date: 3/11/94

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4. UART Transmitter Auto-RTS

The transmitter ready-to-send signal (RTS*) does not function in auto-negate mode (Bit five of the UMR2 register set to one.)

Workaround:

Control RTS*/PortB4 manually. Wait for Transmitter Empty status before negating RTS* (Bit three of the USR register set to one.)

Masks: 0F37 1F37 G57B Date: 3/11/94

5. UART Receiver Auto-RTS

The receiver ready-to-send signal (RTS*) does not function in auto-negate mode (Bit seven of the UMR1 register set to one.)

Workaround:

None. Be sure to check overrun status on receivers (Bit four of the USR set to one.)

Masks: 0F37 1F37 G57B Date: 3/11/94

6. TAS instruction to an 8-bit mode device

If the TAS instruction is used for read-modify-write of an 8-bit mode memory, and the addressed byte is at an even memory location, the read occurs to the even address, but the write back occurs to an odd address i.e. the lsb address bit increments between the read and write.

Workaround:

There are no problems when using the TAS instruction to an odd location on an 8-bit mode device, or odd or even locations of a 16-bit mode device.

Masks: 0F37 1F37 G57B Date: 6/22/94

7. Overlap in chip select ranges

If a programmed chip select address range overlaps an existing chip select range, the higher priority chip select will assert for an access to that range, but it will use the DTACK termination and wait states programmed for the lower priority chip select.

Workaround:

During the access to a common location, one of the overlapping chip selects could be temporarily disabled using the EN bit of the chip select Base Register. Alternatively, different address spaces could be used for the two chip selects to avoid the overlap. If these are not possible, the address decode conflict bit in the System Control Register could be enabled to give a BERR for address conflicts.

Masks: 0F37 1F37 G57B Date: 6/22/94

8. Watchdog Timer refresh

The method of refreshing the watchdog timer by writing to the Watchdog Timer Register (WCR) is unreliable under certain combinations of the watchdog timeout value and refresh write cycle frequency.

Workaround:

Disable and re-enable the watchdog as a refresh mechanism. This involves writing zero to the Watchdog Reference Register (WRR) and then restoring its original value.

Masks: 0F37 1F37 G57B Date: 11/10/94

9. TAS instruction

All TAS instructions cause read-modify-write cycles where the write portion is zero wait states regardless of the chip select programming. The read portion has the correct number of wait states.

Workaround:

None.

Masks: 0F37 1F37 G57B Date: 11/10/95

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10. JTAG TDO line

There is a problem with the drive/tristate control of the TDO signal, during the Extest, Bypass and Idcode modes. Do not use the TDO line.

Workaround:

None.

Masks: 0F37 1F37 Date: 3/21/95

11. Cold Power-On-Reset

The POR circuit may not properly reset the 68307 at the specified minimum V_{CC} of 3.0 V_{DC} when operating at the specified minimum temperature of 0C. The operation at 5.0 volts is not affected.

Workaround:

When operating the device at temperatures below 25C, be sure the V_{CC} does not go below 3.1 V_{DC}.

Masks: 0F37 1F37 Date: 3/21/95

12. M-Bus Multi-Master Arbitration

In systems with multiple I^2C-compatible bus masters, the 68307's M-Bus exhibits problems with arbitration when a master mode START condition is written to the MBCR at the time an alternate master drives SDA low for its start condition. With the exception of this condition, the arbitration procedure functions as specified. Only systems with Multiple I^2C masters may experience this arbitration issue.

Workaround:

a) A documented software workaround exists. Contact your local Motorola sales office for further details.
b) To ensure an alternate master does not have a transfer START at the same time as the 68307 M-Bus master, a software token byte can be passed between the masters to determine which currently has control of the bus.

Masks: 0F37 1F37 G57B Date: 3/21/95

13. Timer Counter Register (TCN1,TCN2)

Writes to the TCNx counter register do not reset the count value. Also, when the timer is brought out of reset (TMRx[0] = 1) the count in TCNx starts from one rather than the expected zero. On reaching the reference count (TRRx register), the restart value is zero as expected.

Workaround:

To reset the TCNx count value (to one), software reset the timer via the TMRx register. The reference (TRRx) and capture registers (TCRx) will also be cleared.

Masks: 0F37 1F37 G57B Date: 8/21/95

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