Cambridge Microprocessor Systems Limited

QuickFire QF-200 Hardware Manual

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1. Introduction

This manual describes the hardware side for the QuickFire QF-200 controller card. This document refers to the MC68VZ328 User Manual, which is supplied as part of this documentation set. Motorola publishes this additional document and they are responsible for the contents of it.

1.1. Features

The QuickFire QF-200 has the following on board features

- MC68VZ328 Processor
- 33 MHz operating speed
- 1 M-byte of flash memory
- 512 k-bytes of battery backed Static RAM
- 1 RS232 serial port
- 1 RS232 / RS485 serial port
- Real time calendar clock
- 2 16-bit timer/counters
- Software watchdog
- 2 SPI interfaces
- 2 PWM interfaces
- Expansion Bus

Expansion devices allow the following features to be added directly to the controller

- Up to 8-M-bytes DRAM
- Up to 8 M-bytes flash memory
- Up to 8 M-bytes static RAM
- Monochrome graphics LCD panels
- Touch screen interface

1.2. Memory Map

The QF-200 memory map is shown below.

	Start Address	End Address	Notes
Flash Memory	$00000000	$000FFFFF	1 M-byte
	$00000000	$001F7FFF	2 M-bytes ❶❷
Peripheral Expansion	$001F8000	$001FFFFF	❷
Static RAM	$00F00000	$00F7FFFF	512 k-bytes
	$00F00000	$00FFFFFF	1 M-byte ❶
Spare	$01000000	$FFFFFEFF	
On board Peripherals	$FFFFF000	$FFFFFFFF	

❶ With expansion memory board fitted
❷ If no external peripherals are used in the PAS area then the full 2 M-byte flash area can be used.

To expand the static RAM to 1 M-byte an 8-bit 512 k-byte RAM device can be fitted to an expansion board. This RAM device can be selected using the signal CSB1 on connector PL2.

To expand the flash memory from 1 M-byte to 2 M-bytes either AMD part number AM29LV800BT or ST part number M29W800AT may be used. If the peripheral expansion memory is not required these devices can be selected using the signal CSA1 on connector PL2. If however the peripheral area is to be used as well then the expansion flash memory should be selected using the MAS signal on PL2.

2. Processor

The heart of the QuickFire QF-200 is the MC68VZ328, one of Motorola's advanced 68000-based micro controllers. This section of the manual will briefly describe the processor function and how it is used on the QF-200. For more details on the processor itself, please refer to the MC68VZ328 User Manual, which is provided as part of this documentation.

The QuickFire QF-200 is designed to make most of the features of the processor available to the user. This includes the following –

- FLX68000 CPU Core
- Chip select logic
- Clock generation module and power control
- Interrupt controller
- General Purpose I/O channels
- Two Pulse Width Modulation (PWM) outputs
- Two general purpose timers
- Two Serial Peripheral Interfaces (SPI)
- Two UARTs
- Liquid Crystal Display (LCD) Controller
- Real time clock (RTC)
- Dynamic Random Access Memory (DRAM)
- Sequential DRAM (SDRAM)

The processor itself has three operating modes. The first, 'Normal' mode is the usual mode of operation for any processor. It allows the controller to run from reset using the standard 68000 vector table and booting the system up using code contained in the on board flash memory. The vast majority of this manual refers to the processor running in this normal mode.

The second mode of operation is 'Emulation' mode. This mode of operation is not used on the QF-200, but if users require this mode of operation, please refer to the MC68VZ328 User Manual where full details are given. Access to the signals required is available on connector PL2 and PL3.

The third mode of operation is 'Bootstrap' mode. This mode allows the processor to run some internal code to allow programs to be downloaded and run using the serial port. For more details on how the QuickFire controller uses the bootstrap mode please refer to section 11.

2.1. FLX68000 CPU

The processor core in the 68VZ328 is identical to the MC68EC000 processor giving full compatibility with 68000 assembler code, 32-bit internal address bus 16-bit data bus and a static design allowing the processor clock to be stopped to provide power saving.

2.2. Chip Select Logic

The 68VZ328 processor provides eight general purpose chip select lines in four banks of two selects. These allow glue less interfacing to a variety of different devices including flash memory, static RAM and DRAM. Each chip select bank can be configured for 8 or 16-bit access, internal or external DTACK generation and write protect options.

The QuickFire QF-200 uses two of the chip select banks, CSA is used to decode the flash memory, CSA0 decoding the on board flash memory and CSA1 being available for expansion flash decoding if required. CSB is used to decode the static RAM. CSB0 is used to decode the on board static RAM device, CSB1 is available for external decoding if required. This chip select can be used to select any type of device with an 8-bit interface.

Chip select banks C and D are not used on the QF-200 itself but will be required if a DRAM expansion is used.

2.3. Clock Generation and Power Saving

The controller uses the clock generation module to provide clock signals to all on chip peripherals using a single 32 kHz oscillator. The output frequency can be adjusted by writing to one of the internal registers although this is not recommended by CMS as changing the frequency of operation will affect the operational status of all the internal modules.

The processor is a static device, which means that it maintains its current status when no clock signals are provided to it. This allows a

number of modes in which the power consumption can be reduced. There are three operating modes ‘Normal’, ‘Doze’ and ‘Sleep’. In ‘Normal’ mode. The processor is clocked all the time. It is the most power hungry mode. In ‘Doze’ mode the processor clock is suspended for a period of time during which the power consumption is reduced. A register setting determines how long the clock is off for each period. In ‘Sleep’ mode the processor clock is suspended until an external event occurs which wakes the processor up. In both doze and sleep mode the real time clock and DRAM are refreshed to maintain data. Sleep mode offers the lowest power consumption.

Also to reduce power consumption unused modules can be disabled (please refer to individual module descriptions for full details) and internal pull up / pull down resistors can be disabled.

2.4. Interrupt Controller

The interrupt controller module in the MC68VZ328 provides an interface between all the on chip peripheral interrupt sources and the external level and edge triggered interrupt inputs.

The interrupt controller receives each interrupt request and then prioritises it to one of seven levels. Level 7 interrupts have the highest priority, while level 1 interrupts have the lowest priority. When an interrupt is received the interrupt controller generates an interrupt request to the CPU. The CPU receives the interrupt request and generates an interrupt acknowledge cycle when the current instruction is completed. The interrupt controller places the vector number of the highest priority interrupt currently pending on the CPU bus. The CPU then services that interrupt by running the code in the interrupt service routine.

The interrupt controller in the MC68VZ328 controller provides one vector for each of the seven interrupt levels. On the QuickFire controllers the user vectors all start with $4x, where the most significant nibble is programmed into the Interrupt Vector Register and the least significant three bits are the interrupt level.

The following is a list of interrupt sources on the QuickFire QF-200 giving details of the associated module and the interrupt level. Where the interrupt level is configurable this is done using the Interrupt Level Register.

Description	Level	Associated Module
EMUIRQ or hardware breakpoint interrupt	7	Emulator
IRQ6 external interrupt	6	Interrupt Controller
Timer 1	6	Timers
Timer 2	Configurable 1 to 6	Timers
Pulse Width Modulator 1	6	PWM
Pulse Width Modulator 2	Configurable 1 to 6	PWM
IRQ5 external interrupt	5	Interrupt Controller
Serial Peripheral Interface 1	Configurable 1 to 6	SPI
Serial Peripheral Interface 2	4	SPI
UART 1	4	Serial Port
UART 2	Configurable 1 to 6	Serial Port
Software Watchdog Timer	4	Real Time Clock
Real Time Clock	4	Real Time Clock
Real Time interrupt	4	Real Time Clock
Keyboard interrupt	4	Interrupt Controller
INT3 general purpose interrupt	4	Interrupt Controller
INT2 general purpose interrupt	4	Interrupt Controller
INT1 general purpose interrupt	4	Interrupt Controller
INT0 general purpose interrupt	4	Interrupt Controller
IRQ3 external interrupt	3	Interrupt Controller
IRQ2 external interrupt	2	Interrupt Controller
IRQ1 external interrupt	1	Interrupt Controller

For more details on the interrupt controller please refer to the MC68VZ328 User Manual. For details on how to write interrupt service

routines please refer to your language User Manual and the accompanying example programs.

2.5. General Purpose I/O channels

The MC68VZ328 controller has up to 76 general purpose I/O channels over 12 ports. All of these have alternative special function capacities. Depending on which features of the controller the application required determines how many channels are available for a particular application. Some of the channels are used for special functions on the QuickFire QF-200, for details of this usage please refer to section 10 of this manual.

2.6. Pulse Width Modulation (PWM) outputs

There are two PWM ports on the MC68VZ328 controller. Each port can operate in one of three modes, playback, tone or digital to analogue conversion.

PWM unit 1 has an 8-bit resolution, while the second unit has a resolution of 16-bits. The pulse width modulator unit has two output signals. PWMO1 is generated by combining the outputs of both PWM1 and PWM2, the combination depends on the value placed in the Peripheral Control Register. The second output PWMO2 is generated by the output of PWM2.

PWM unit 1 is clocked using either the SYSCLK or CLK32 signal. This can then be divided down using a prescaler register. The second unit is clocked solely with the SYSCLK signal. Again this can be divided down using a prescaler value.

For more details on the PWM module please refer to the MC68VZ328 User Manual.

2.7. General Purpose timers

The MC68VZ328 controller has two 16-bit counter / timers. On the QuickFire QF-200 timer 1 is used to generate periodic interrupts for

the Minos task switching. It is not recommended that this timer is used for anything else. Timer 2 is available for use by the application.

Both timers share an external pin, PB6/TIN/TOUT. If this channel is programmed as a special function I/O it can also be configured as an input, in which case it can be used as a clock source or the edge detect input for the capture registers. The operating system does not use this pin so it is available for the application to use with timer 2 if required.

Both timers have an identical register set. Each timer consists of a clock source and prescaler, a counter module and a capture module. The clock source fro each timer can be selected from one of four sources, SYSCLK, SYSCLK/16, CLK32 and TIN, the external input pin. The prescaler allows the selected clock input signal to be divided down by up to 256, allowing the maximum period of 512 seconds. Of the four clock sources only CLK32 is available while the processor is in sleep mode. If this signal is selected the processor can be woken up after a selected time period using one of the timers.

The timer compare feature allows an interruptible event to be generated when the timer counter value reaches the value programmed into the timer compare register. Depending on the configuration, when the compare value is reached the timer can either restart from 0 or continue running.

The timer capture feature allows the current value of the timer to be stored when a falling edge, a rising edge or any edge occurs on the TIN pin. An interrupt can also be generated on this event if required.

2.8. Serial Peripheral Interfaces (SPI)

The MC68VZ328 controller has two serial peripheral interface ports. The QuickFire QF-200 does not use either of these ports but they are made available for external access. The SPI ports allow a range of peripheral devices to be connected to the controller.

SPI port 1 can operate as both a master device and a slave device, while SPI port 2 can only operate in master mode only. For more details please refer to the MC68VZ328 User Manual.

2.9. Serial Module

The MC68VZ328 has two universal asynchronous serial ports (UART). Serial port 2 is an enhanced version of serial port 1 with larger FIFO buffers.

Both serial ports on the QuickFire QF-200 are fitted with RS232 buffers to allow communication with external devices using this serial format in the default settings. RS232 communication is commonly used to connect two devices together over a short distance. The RS232 ports on the QuickFire are both configured for connection directly to a PC type device (Data Terminal Equipment DTE) so operate as Data Communication Equipment (DCE). If the serial port is required to operate in the alternative format a null modem will be required that crosses over the RXD / TXD and RTS / CTS connections. The RS232 Minos drivers supplied as standard with the development packages require the handshaking lines to be connected. If the application does not use RTS/CTS handshaking then the pins on the serial connectors should be connected together.

UART1 is also fitted with an RS485 half duplex transceiver. RS485 is a balanced differential interface that enables reliable data communication in noisy environments. To select to receive data from the RS485 device LK4 (section 9.4) should be fitted in the South position. When the serial port is receiving data from the RS485 port, data is transmitted on both the RS485 and RS232 (TXD) outputs. A different software driver (rts328) is required to operate the serial port in RS485 mode, as the RTS line is used to operate the tristate control for the transceiver device. When power is applied to the QuickFire the RS485 receiver is enabled, allowing the controller to listen for activity on the transmission line. When the controller has data to transmit, the receiver is turned off and the transmitter is enabled. Once the data has been sent out the transmitter is disabled and the receiver enabled again. A software protocol should be employed to ensure that only

one controller on the RS485 bus is writing data at a time, otherwise the data on the RS485 network will get corrupted. Efficient communication over RS485 relies on a correctly terminated transmission line. If the controller is at either end of the transmission line a terminator must be fitted to compensate for the line impedance. To enable this to be done easily, a terminating resistor of 100Ω is fitted to the QuickFire controller. To enable the terminating resistor simply fit a jumper on link LK6 (section 9.6). To disable the terminator, remove the jumper.

2.9.1. Serial Port Buffers

The serial line drivers and receivers used on the QuickFire controller are designed to generate the required signalling voltages for the serial interface from the single 3 Volt supply.

The RS232 buffers used have internal charge pumps to generate the minimum +/- 5 volt output swings. Both devices operate in a shutdown mode, where if there is not any valid receiver input and there is not a valid edge on either the receivers or transmitters for 30 seconds the devices shut down to conserve power. The device is woken up immediately there is a valid RS232 level on one of the receiver inputs. This means that if there is not a cable connected to the serial port the buffer will always be in shutdown mode. If the serial ports are always connected to valid RS232 levels, the serial buffers can still be enabled to operate in shutdown mode by breaking the resistor link (R25 for serial port 1 and R32 for serial port 1) and connecting the resistor to the other option. In this mode the buffers will shutdown when there has been not data received or sent within 30 seconds. In this mode the will be a short delay while the buffer enables. When the RS232 serial buffers are shutdown, the current consumption is typically 1μA as opposed to the typical operating current of 0.3mA.

The RS485 buffer will typically consume 1.6μA while it is in receive mode and 50μA while the driver is operating.

2.10. Liquid Crystal Display (LCD) Controller

The QuickFire QF-200 board does not support liquid crystal displays directly, but they can be added as required. We would recommend adding additional memory to the controller if the LCD is required as the LCD controller shares conventional system memory for the video memory. For the full display 256 k-bytes of memory is required.

The LCD controller supports monochrome graphics LCD panels up to a maximum size of 640 x 512 pixels. It can display 16 simultaneous different grey scales from a palette of 16 density levels. Using one of the SPI ports the controller can interface directly to touch panels and using one of the PWM outputs the LCD contrast can be adjusted under program control. For more details please refer to the MC68VZ328 User Manual.

2.11. Real time clock (RTC)

The real time clock module is made up with six blocks. The real time clock can generate eight different interrupts to the processor. Each interrupt can be enabled or disabled as required. The eight interrupt sources are shown in the table below.

Interrupt Name	Interrupt Controller	Resolution
Real Time Interrupt	Real Time Interrupt	Eight different rates
Stopwatch	Real Time Clock	Minutes
1HZ	Real Time Clock	Seconds
MIN	Real Time Clock	Minutes
HR	Real Time Clock	Hours
DAY	Real Time Clock	Days
ALM	Real Time Clock	Seconds
Watchdog	Watchdog	Minutes

The first block is the prescaler. This takes the CLK32 signal from the phase locked loop and divides this signal down to produce a 1 Hz clock which is used to clock all other modules in the real time clock. The CLK32 signal is always available even when the controller is in a

low power mode. This ensures that the real time clock keeps the correct value even when the main power to the board is removed.

The time of day counters consists of four counter registers that are incremented by the 1HZ clock signal from the prescaler. The four counters are; the second counter (6 bits), the minute counter (6 bits), the hours counter (5 bits) and the day counter (9 bits). The time counters are located in the RTCTIME register and the day counter is stored in its own register. The clock can count up to 512 days. The register values are not limit checked so if an illegal value is written to the registers, they will keep that value until the counter feeding the register rolls over. For example if the value 26 is written to the hours counter, it will retain this incorrect value until the minute counter rolls over when the hour counter will be reset back to 0. Each of the four counters can be enabled to generate an interrupt when the counter rolls over. When the second counter increments from 59 to 00, it can generate a MIN interrupt, when the minute counter rolls over a HR interrupt can be generated etc.

The alarm module consists of copies of the time of day counters. When the time of day counters equal the values programmed into the alarm registers an alarm event occurs. An alarm event can be programmed to generate an interrupt to the processor. If the alarm is not disabled an alarm will be repeated every 24 hours. If a single alarm event is required the service routine for the alarm should disable the alarm before it finishes.

The real time interrupt timer offers an additional interrupt source. The period of the interrupt can be configured to one of eight predetermined frequencies between 4 Hz and 512 Hz, please refer to the MC68VZ328 User Manual for details on setting the frequency for this interrupt.

The minute stopwatch, when it is enabled, provides a counter with a one minute resolution. When the counter value decrements down to –1 an interrupt can be generated. As the stopwatch is incremented with the minute counter the first minute can be short depending on how many seconds had elapsed when the stopwatch is enabled.

The real time clock module provides a watchdog timer for the MC68VZ328 controller. The watchdog can be used to confirm that the processor is running correctly. When the watchdog is enabled the processor must access the watchdog register within each two-second interval to prevent the watchdog timing out. If the watchdog times out it can be programmed to generate either an interrupt or a system reset. The watchdog is clocked using the 1HZ signal that means that this timer has a 1 second resolution.

2.12. Dynamic Random Access Memory (DRAM)

The QuickFire QF-200 board does not make use of the DRAM controller part of the MC68VZ328 controller but it s available for user expansion if required.

The DRAM controller provides a glueless interface to 8-bit or 16-bit DRAM. It supports EDO, Fast Page Mode and synchronous DRAM with a programmable refresh rate. It allows up to 32 M-bytes of DRAM to be added directly to the processor.

The DRAM controller uses two of the chip select banks group C and group D. Both of these chip select groups are not used on the standard QuickFire QF-200 to allow the DRAM to be used unrestricted if required. For more details on the DRAM controller please refer to the MC68VZ328 User Manual.

2.13. Registers

The table below lists all the registers in the MC68VZ328 controller. The page number given refers to the MC68VZ328 User Manual where a full description of the register can be found. The register addresses are given assuming that the controller is being used in its default state when supplied by CMS.

Great care must be taken when accessing the chip registers as writing incorrect values to the registers can cause serious problems with your

controller. Register addresses not shown below are reserved and should not be accessed.

Address	Width	Abbreviation	Name	Page
$FFFFF000	8	SCR	System Control	5-2
$FFFFF003	8	PCR	Peripheral Control	5-4
$FFFFF004	32	IDR	Silicon ID	5-5
$FFFFF008	16	IODCR	I/O Drive Control	5-6
$FFFFF100	16	CSGBA	Chip Select Group A Base	6-4
$FFFFF102	16	CSGBB	Chip Select Group B Base	6-4
$FFFFF104	16	CSGBC	Chip Select Group C Base	6-4
$FFFFF106	16	CSGBD	Chip Select Group D Base	6-4
$FFFFF108	16	CSUGBA	Chip Select Upper Group Address	6-6
$FFFFF10A	16	CSCR	Chip Select Control	6-16
$FFFFF110	16	CSA	Group A Chip Select	6-8
$FFFFF112	16	CSB	Group B Chip Select	6-8
$FFFFF114	16	CSC	Group C Chip Select	6-8
$FFFFF116	16	CSD	Group D Chip Select	6-8
$FFFFF118	16	EMUCS	Emulation Chip Select	6-16
$FFFFF200	16	PLLCR	PLL Control	4-8
$FFFFF202	16	PLLFSR	PLL Frequency Select	4-10
$FFFFF207	8	PCTLR	Power Control	4-14
$FFFFF300	8	IVR	Interrupt Vector	9-7
$FFFFF302	16	ICR	Interrupt Control	9-8
$FFFFF304	32	IMR	Interrupt Mask	9-10
$FFFFF30C	32	ISR	Interrupt Status	9-12
$FFFFF310	32	IPR	Interrupt Pending	9-16
$FFFFF314	16	ILCR	Interrupt Level Control	9-19
$FFFFF400	8	PADIR	Port A Direction	10-6

$FFFFF401	8	PADATA	Port A Data	10-6
$FFFFF402	8	PAPUEN	Port A Pull-up Enable	10-6
$FFFFF408	8	PBDIR	Port B Direction	10-8
$FFFFF409	8	PBDATA	Port B Data	10-8
$FFFFF40A	8	PBPUEN	Port B Pull-up Enable	10-8
$FFFFF40B	8	PBSEL	Port B Select	10-8
$FFFFF410	8	PCDIR	Port C Direction	10-11
$FFFFF411	8	PCDATA	Port C Data	10-11
$FFFFF412	8	PCPDEN	Port C Pull-down Enable	10-11
$FFFFF413	8	PCSEL	Port C Select	10-11
$FFFFF418	8	PDDIR	Port D Direction	10-16
$FFFFF419	8	PDDATA	Port D Data	10-16
$FFFFF41A	8	PDPUEN	Port D Pull-up Enable	10-16
$FFFFF41B	8	PDSEL	Port D Select	10-16
$FFFFF41C	8	PDPOL	Port D Polarity	10-16
$FFFFF41D	8	PDIRQEN	Port D Interrupt Request Enable	10-16
$FFFFF41E	8	PDKBEN	Port D Keyboard Enable	10-16
$FFFFF41F	8	PDIRQEG	Port D Interrupt Request Edge	10-16
$FFFFF420	8	PEDIR	Port E Direction	10-21
$FFFFF421	8	PEDATA	Port E Data	10-21
$FFFFF422	8	PEPUEN	Port E Pull-up Enable	10-21
$FFFFF423	8	PESEL	Port E Select	10-21
$FFFFF428	8	PFDIR	Port F Direction	10-24
$FFFFF429	8	PFDATA	Port F Data	10-24
$FFFFF42A	8	PFPUEN	Port F Pull-up/Pull-down Enable	10-27
$FFFFF42B	8	PFSEL	Port F Select	10-27
$FFFFF430	8	PGDIR	Port G Direction	10-28
$FFFFF431	8	PGDATA	Port G Data	10-28
$FFFFF432	8	PGPUEN	Port G Pull-up Enable	10-30
$FFFFF433	8	PGSEL	Port G Select	10-31
$FFFFF438	8	PJDIR	Port J Direction	10-31

$FFFFF439	8	PJDATA	Port J Data	10-32
$FFFFF43A	8	JPUEN	Port J Pull-up Enable	10-33
$FFFFF43B	8	PJSEL	Port J Select	10-33
$FFFFF440	8	PKDIR	Port K Direction	10-34
$FFFFF441	8	PKDATA	Port K Data	10-35
$FFFFF442	8	PKPUEN	Port K Pull-up/Pull-down Enable	10-36
$FFFFF443	8	PKSEL	Port K Select	10-36
$FFFFF448	8	PMDIR	Port M Direction	10-37
$FFFFF449	8	PMDATA	Port M Data	10-38
$FFFFF44A	8	PMPUEN	Port M Pull-up Enable	10-39
$FFFFF44B	8	PMSEL	Port M Select	10-40
$FFFFF500	16	PWMC1	PWM1 Control	15-4
$FFFFF502	16	PWMS1	PWM1 Sample	15-6
$FFFFF504	8	PWMP1	PWM1 Period	15-7
$FFFFF505	8	PWMCNT1	PWM1 Counter	15-7
$FFFFF510	16	PWMC2	PWM2 Control	15-8
$FFFFF512	16	PWMS2	PWM2 Sample	15-9
$FFFFF514	16	PWMP2	PWM2 Period	15-10
$FFFFF516	16	PWMCNT2	PWM2 Counter	15-10
$FFFFF600	16	TCTL1	Timer 1 Control	12-6
$FFFFF602	16	TPRER1	Timer 1 Prescaler	12-8
$FFFFF604	16	TCMP1	Timer 1 Compare	12-9
$FFFFF608	16	TCN1	Timer 1 Counter	12-10
$FFFFF60A	16	TSTAT1	Timer 1 Status	12-12
$FFFFF610	16	TCTL2	Timer 2 Control	12-6
$FFFFF612	16	TPRER2	Timer 2 Prescaler	12-8
$FFFFF614	16	TCMP2	Timer 2 Compare	12-9
$FFFFF618	16	TCN2	Timer 2 Counter	12-10
$FFFFF61A	16	TSTAT2	Timer 2 Status	12-12
$FFFFF700	16	SPIRXD1	SPI 1 Receive Data	13-4
$FFFFF702	16	SPITXD1	SPI 1 Transmit Data	13-5
$FFFFF704	16	SPICONT1	SPI 1 Control / Status	13-6
$FFFFF706	16	SPIINTCS	SPI 1 Interrupt Control / Status	13-8

$FFFFF708	16	SPITEST	SPI 1 Test	13-10
$FFFFF70A	16	SPISPC	PSI 1 Sample Period Control	13-11
$FFFFF800	16	SPIDATA2	SPI 2 Data	13-14
$FFFFF802	16	SPICONT2	SPI 2 Control / Status	13-15
$FFFFF900	16	USTCNT1	UART 1 Status / Control	14-10
$FFFFF902	16	UBAUD1	UART 1 Baud Control	14-12
$FFFFF904	16	URX1	UART 1 Receiver	14-13
$FFFFF906	16	UTX1	UART 1 Transmitter	14-14
$FFFFF908	16	UMISC1	UART 1 Miscellaneous	14-16
$FFFFF90A	16	NIPR1	UART 1 Non –integer Prescaler	14-18
$FFFFF910	16	USTCNT2	UART 2 Status / Control	14-10
$FFFFF912	16	UBAUD2	UART 2 Baud Control	14-12
$FFFFF914	16	URX2	UART 2 Receiver	14-13
$FFFFF916	16	UTX2	UART 2 Transmitter	14-14
$FFFFF918	16	UMISC2	UART 2 Miscellaneous	14-16
$FFFFF91A	16	NIPR2	UART 2 Non –integer Prescaler	14-18
$FFFFF91C	16	HMARK	UART 2 FIFO Half Mark	14-29
$FFFFFA00	32	LSSA	LCD Screen Start Address	8-10
$FFFFFA05	8	LVPW	LCD Virtual Page Width	8-11
$FFFFFA08	16	LXMAX	LCD Screen Width	8-12
$FFFFFA0A	16	LYMAX	LCD Screen Height	8-12
$FFFFFA18	16	LCXP	LCD Cursor X Position	8-12
$FFFFFA1A	16	LCYP	LCD Cursor Y Position	8-13
$FFFFFA1C	16	LCWCH	LCD Cursor Width & Height	8-14

$FFFFFA1F	8	LBLKC	LCD Blink Control	8-14
$FFFFFA20	8	LPICF	LCD Panel Interface Configuration	8-15
$FFFFFA21	8	LPOLCF	LCD Polarity Configuration	8-16
$FFFFFA23	8	LACDRC	LCD Rate Control	8-16
$FFFFFA25	8	LPXCD	LCD Pixel Clock Divider	8-17
$FFFFFA27	8	LCKCON	LCD Clocking Control	8-18
$FFFFFA29	8	LRRA	LCD Refresh Rate Adjustment	8-18
$FFFFFA2D	8	LPOSR	LCD Panning Offset	8-19
$FFFFFA31	8	LFRCM	LCD Frame Rate Control Modulation	8-19
$FFFFFA33	8	LCPMR	LCD Grey Palette Mapping	8-20
$FFFFFA36	8	PWMR	PWM Contrast Control	8-20
$FFFFFA38	8	RMCR	Refresh Mode Control	8-21
$FFFFFA39	8	DMACR	DMA Control	8-22
$FFFFFB00	32	RTCTIME	RTC Time of Day	11-3
$FFFFFB04	32	RTCALRM	RTC Alarm	11-3
$FFFFFBOA	16	WATCHDOG	Watchdog Timer	11-4
$FFFFFBOC	8	RTCCTL	RTC Control	11-10
$FFFFFB0E	16	RTCISR	RTC Interrupt Status	11-10
$FFFFFB10	16	RTCIENR	RTC Interrupt Enable	11-12
$FFFFFB12	8	STPWCH	Stopwatch Minutes	11-14
$FFFFFB1A	16	DAYR	RTC Day Count	11-6
$FFFFFB1C	16	DAYALARM	RTC Day Alarm	11-8
$FFFFFC00	16	DRAMMC	DRAM Memory Configuration	7-12
$FFFFFC02	16	DRAMC	DRAM Control	7-14
$FFFFFC04	16	SDCTRL	SDRAM Control	7-16
$FFFFFC06	16	SDPWDN	SDRAM Power Down	7-18
$FFFFFD00	32	ICEMACR	ICEM Address Compare	16-4

$FFFFFD04	32	ICEMAMR	ICEM Address Mask	16-4
$FFFFFD08	16	ICEMCCR	ICEM Control Compare	16-6
$FFFFFD0A	16	ICEMCMR	ICEM Control Mask	16-6
$FFFFFD0C	16	ICEMCR	ICEM Control	16-8
$FFFFFD0E	16	ICEMSR	ICEM Status	16-10
$FFFFFExx		Boot	Bootloader Microcode Space	

3. Flash Memory

The QuickFire QF-200 has 1 M-byte of on board programmable flash memory fitted. The memory is configured as 512 k-bytes x 16-bits wide. The on board flash memory is divided up into 19 sectors of varying sizes. Please refer to the table below, which shows the sector number, sector address and sector size. The operating system and default utility programs reside in the first three sectors, taking up 192 k-bytes. The remainder of the on board flash is available for application use and storage. The flash memory should be used in sectors as shown. Before writing new data to a sector, the whole sector must be erased first, this means that the data in the selected sector will be lost unless a copy is made first.

Sector Number	Size (k-bytes)	Address Range	
		Start	End
0	64	$00000000	$0000FFFF
1	64	$00010000	$0001FFFF
2	64	$00020000	$0002FFFF
3	64	$00030000	$0003FFFF
4	64	$00040000	$0004FFFF
5	64	$00050000	$0005FFFF
6	64	$00060000	$0006FFFF
7	64	$00070000	$0007FFFF
8	64	$00080000	$0008FFFF
9	64	$00090000	$0009FFFF
10	64	$000A0000	$000AFFFF
11	64	$000B0000	$000BFFFF

12	64	$000C0000	$000CFFFF
13	64	$000D0000	$000DFFFF
14	64	$000E0000	$000EFFFF
15	32	$000F0000	$000F7FFF
16	8	$000F8000	$000F9FFF
17	8	$000FA000	$000FBFFF
18	16	$000FC000	$000FFFFF

The smaller sized sectors at the top of the flash memory are ideal for storing default set up and configuration data for the application program as they are small and can easily be updated by copying, changing and then rewriting the new data without affecting other areas of the flash memory. If used in this manner there are 768 k-bytes available for application program storage and 64 k-bytes available for data storage.

During normal operation the on board flash memory is selected using CSA0. If a QuickFire FlashFormatter card is used then the FORM/STORE switch on the FlashFormatter will determine which device is selected. If the switch is set to STORE then the on board flash memory will be decoded using CSA0 and the expansion memory using CSA1. If the switch is set to FORM, then the on board Flash memory is decoded using CSA1 and the expansion memory is decoded using CSA0.

An additional 1 M-byte of flash memory can be added to the QuickFire QF-200 using an identical part to that on the QF-200 board and selecting it using the CSA1 signal on connector PL2. If the application requires the decoding of the Peripheral Address area, then the signal MAS should be used to select the expansion flash memory. In this case the upper 32 k-byte of the expansion flash memory will not be accessed as this area will clash with the Peripheral Address space. The MAS signal takes this memory clash into account. Compatible flash memory devices are as follows –

Manufacturer	Bottom boot block	Top boot block
ST Microelectronics	M29W800AB	M29W800AT

AMD	AM29LV800BB	AM29LV800BT

Bottom boot block devices have the smaller sector sizes in the bottom sectors, top boot block devices have the smaller sector sizes in the top sectors as on the QuickFire controllers. The operating system and library code supports the above devices only. If other devices are used additional software routines will be required to write and erase the flash memory in system. Parts will access times of 90 ns or faster should always be used.

4. Static RAM

The QuickFire QF-200 has 512 k-bytes of battery backed static RAM fitted. The on board RAM is configured as 512 k-bytes x 8-bit. This RAM is decoded using CSB0 to operate between $00F00000 and $00F7FFFF. The RAM is powered from a battery backed power supply, so that the contents of the RAM can be kept while the board is not powered. The RAM can be cleared by moving link LK5 while the power is removed from the controller card. Please see section 9.5 for details, this should never be done when the controller is powered up.

The on board RAM can be expanded to 1 M-byte using a memory expansion card. The additional RAM should be of the same type as that fitted to the QuickFire controller. The extra memory can be selected using the chip select signal CSB1. This chip select decodes memory in the area $00F80000 to $00FFFFFF. If the extra memory is required to be battery backed a separate battery supply will be required.

The operating system partitions the on board RAM into two blocks. The split is determined by a setting in the merge file when the on-board flash is generated. The default is 256 k-bytes. The lower block (by default $00F00000 to $00F3FFFF) is reserved from the operating system and is used to download C programs into. By default all C programs are linked to load into this address range when they are compiled for RAM. The upper block (by default $00F40000 to

$00FFFFFF) is defined as operating system space. It is this upper area that is used to claim buffers, data modules, stacks and other system use.

5. Voltage Regulator

The QuickFire QF-200 board is fitted with a low power voltage regulator. This device is enabled using link LK3 (refer to section 9.3) and link LK2 should be adjusted accordingly. The device takes the Vin voltage supplied to the board from either the expansion bus connectors or the screw terminals and converts the voltage to 3.0 Volts for use on the board. The input to the voltage regulator can be up to 16 volts but we would not recommend powering the board with greater than 6 Volts to prevent the on board battery being over charged.

The voltage regulator is capable of generating a supply voltage in the range 2.9416 – 3.084 volts at a current of up to 200 mA. This is sufficient to power the controller card and a number of peripheral cards. When the device is disabled it draws less that 1 μA.

6. Expansion

The QuickFire QF-200 has two expansion bus connectors and a digital I/O bus connector. The local expansion bus allows peripheral and memory expansion boards to be mounted directly on the QuickFire controller. This is ideal if a single expansion board is required. The ‘Module Bus’ expansion board will allow the controller to be used in a racking type system where the expansion cards are plugged into a back plane. For details of the connectors please refer to section 12.3 for the local expansion connector, section 12.4 for the ‘Module Bus’ expansion connector and section 12.2 for the Digital I/O bus connector.

6.1. Local Bus Expansion

The Local Bus expansion connector is a 64 way ab DIN41612 vertical plug. For details of the connections on this connector please refer to section 12.3.

6.1.1. Data Bus (D0 – D15)

These signals form the 68000 data bus. They are used to transfer data from one address to the other. The data is valid on the data bus when DS0 (D0 – D7) is low and when DS1 (D8 – D15) is low. For normal 68000 peripherals, if the device is an 8-bit device the device should be connected to the upper half of the data bus and the address lines are offet by 1 (A0 is not used). The peripheral is then addressed at odd addresses, using the 68000 machine code instruction movep, if required. An exception to this rule is when the processor makes use of dynamic bus sizing when using a programmed chip select. If the chip select is selected as an 8-bit chip select then the peripheral must be connected to the lower half of the address bus and it is addressed sequentially. This mode of operation is used for the RAM on the QuickFire using CSB0 and CSB1. Peripherals selected using the PAS strobe must be connected using the upper data bus only. The data bus is pulled high on the QuickFire contoller.

6.1.2. Address Bus (A0 – A23)

This is the 68000 Address bus. It is used for selecting the address at which the data is to be read or written. Normally for 68000 processors A0 is not used and A1 is the least significant address line. The data strobes DS0 and DS1 are used to select whether it is the upper or lower byte that is being accessed. This is not true when the processor is using a chip select programmed as an 8-bit select, when A0 becomes the least significant address line. The MC68VZ328 has a total of 32 address lines for internal computation but only the least significant 24 of these are available for external use.

6.1.3. Data Strobes (DS0, DS1)

The two data strobes are used to validate data on the data bus. If DS0 is low then the data on signals D0 – D7 is valid and the odd byte is accessed. If DS1 is low then the data on signals D8 – D15 is valid and the even byte is accessed. For 16-bit accesses both data strobes will be driven low by the processor. While both of the data strobes are high no data is valid. Both of the data strobes are pulled high on the QuickFire controller.

6.1.4. Peripheral Address Strobe (PAS)

The peripheral address strobe is used to select the peripheral area. When a valid address is accessed within the memory range $001F8000 to $001FFFFF the PAS signal will go low. This can be used to simplify the decoding of peripherals, which only need to decode from A14 downwards, rather than the whole address bus. While this signal is high no external peripherals will be selected. On the QuickFire QF-200 the PAS strobe is generated to occupy the upper 32 k-bytes of CSA1. Once the address strobe has gone low the processor will wait for a data acknowledgement (DTACK – see section 6.1.9) before continuing. The PAS signal is pulled high on the QuickFire controller.

6.1.5. Address Strobe (AS)

The address strobe is used to validate the address bus. When the address bus has a valid address on it, the address strobe signal goes low to indicate that the device currently being addressed is should be selected. The MC68VZ328 does not have an external address strobe, so on the QuickFire QF-200 the address strobe decoded using CSA1. The address strobe will go low if a valid address is accessed between $00100000 to $001F7FFF. Once this signal has gone low the processor will wait for a data acknowledgement (DTACK – see section 6.1.9) before continuing. The address strobe signal is pulled high on the QuickFire controller.

6.1.6. Reset

The reset signal is a bi directional signal that can be used to generate a hardware reset to the system. Devices connected to the expansion bus can pull the reset line low to generate a system reset, or they can be reset if this signal is low. The reset signal is pulled up on the processor card under normal operation. When the supply power to the controller card fails and the MC68VZ328 is being powered by the on board battery, this signal will be low.

6.1.7. Clock Output (CLK)

This signal is the external clock output from the processor. It is used to synchronise external devices to the processor. The clock signal on the QuickFire QF-200 operates at a frequency of 33 MHz, and it should always be enabled.

6.1.8. Read / Write (R/W)

The Read/Write signal on the expansion connector determines whether the processor is reading data from a peripheral or writing data to it. If the read/write line is high during an access, data is read from the device being accessed. If it is low, then data is written to the device.

6.1.9. Data Acknowledge (DTACK)

The 68000 is an asynchronous processor. Once a device has been accessed the processor will wait until the data is ready from the device before proceeding to the next instruction. The DTACK signal is used to inform the processor that the peripheral has completed it operation and the processor can continue. The DTACK signal is normally high, when active it should be pulled low using an open collector driver to signal completion using a wired-or arrangement.

Some of the MC68VZ328 chip select areas use an automatically generated DTACK after a programmed number of wait states. When using these memory areas an external DTACK is not required. On the

QuickFire QF-200 this applies only to RAM expansion using CSB1, all other areas will require a DTACK to be generated.

6.1.10. I²C Control (SCL, SDA)

These two signals are not used on the QuickFire QF-200, which does not support the I²C bus. There is no connection to these pins.

6.1.11. Interrupts (IRQ6, IRQ5, IRQ3, IRQ2, NMI)

All interrupt inputs on the expansion bus should be driven using open collector drives. This allows the interrupts to function as wired-or, where a number of different devices can pull the same interrupt line low. All the external interrupts on the QuickFire. Under normal operation all the interrupt inputs are active low and are level sensitive. IRQ6, IRQ3 and IRQ2 can be programmed to be active high and edge sensitive if required, but this may make the controller incompatible with some expansion cards that would expect the interrupts to be active low as on a standard 68K based system. The QuickFire QF-200 does not support the NMI interrupt and there is not any connection to this pin.

6.1.12. Volt Supplies (VCC, GND, -12, +12)

These four signals are the power supply signals to peripheral devices. –12 and +12 are voltages commonly used to operate relays and other mechanical devices. The QuickFire QF-200 does not use either of these supplies and there are not any connections made to these pins.

The GND signal is the common supply for the controller. All voltages on the controller are referenced to this supply signal.

The VCC signal can be one of two signals depending on the setting of LK7. If LK7 is fitted in the North position, then the VCC on the expansion connectors is the 3 Volt supply from the QuickFire controller. If the link is fitted South, then the VCC signal will be the input power supply to the QuickFire controller. This could be up to 5 Volts if the on board regulator is being used to generate the logic 3 Volt supply. Care must be taken to ensure that the link is fitted in the

required position otherwise higher voltages could damage devices fitted to expansion cards.

6.2. Module Bus Expansion

The only signal difference between the Local Bus Expansion (section 6.1) and the Module Bus expansion is that the IACK signal on the Module Bus connector is connected to the 3 Volt power supply. This is to allow back plane based peripherals that use IACK chaining to function correctly.

The Module Bus expansion connector is a 64 way ab DIN41612 90 degree plug. For details of the connections on this connector please refer to section 12.4.

6.3. Digital I/O Expansion

The Digital I/O expansion connector is a 64 way ab DIN41612 vertical plug. For details of the connections on this connector please refer to section 12.2.

6.3.1. Write Enables (UWE, LWE)

These two signals, both active low, indicate a write cycle is in progress. If UWE is low then the upper data byte is being written, if LWE is low then the lower data byte is being written. The UWE signal should be used as the WE input to an expansion RAM if the device is selected using the CSB1 chip select signal. Neither of these signals can be used as general purpose I/O channels.

6.3.2. Output Enable (OE)

This active low signal is used to enable the output buffers of the on board flash and static RAM. It can not be used as a general I/O channel

6.3.3. Device Selects (MAS, PAS, CSA1, CSB1)

These four device select signals can be used to select external peripherals or memory. All these signals are active low. For a description of the PAS signal please refer to section 6.1.4. The MAS signal is the same as the AS signal on the expansion bus (section 6.1.5).

CSA1 is the upper half of the decoded area assigned to the flash memory. If no external peripheral devices are required, this chip select signal can be used to select an external flash memory to expand the flash up to 2 M-bytes (please refer to section 3 for more details).

CSB1 is the upper half of the decoded area assigned to the static RAM. This chip select can be used to select a second RAM device or external peripheral if required. It is configured as an 8-bit chip select with an automatically generated DTACK signal.

6.3.4. Receive Data (RXD1, RXD2)

These two signals are the logic level receiver inputs for the two serial ports.

6.3.5. Transmit Data (TXD1, TXD2)

These two signals are the logic level transmitter outputs for the two serial ports.

6.3.6. Handshaking lines (RTS1, RTS2, CTS1, CTS2)

These four signals are the logic level handshaking lines for the two serial ports. If serial port 2 is being used in RS485 mode the RTS signal is used as the tristate control for the RS485 transceiver device.

6.3.7. Mode Select (MODE)

This is a special function for channel PD0. When the controller starts up the ‘shell’ utility program checks the status of this channel to determine if the default terminal shell is run or a user defined turnkey

program is run. Once the controller is running this channel can be used as a general purpose I/O channel with interrupt capability. If the channel is held low when the 'shell' program runs then a turnkey program will be ran if one exists.

6.3.8. Manual Reset (MR)

The manual reset signal is connected in parallel to the reset button on the QuickFire controller. It will allow an external device to reset the controller by pulling this channel low. While this signal is low the processor will be held in its reset state, it will not start running until the channel is released. It is pulled up on the controller by a resistor.

6.3.9. Input Power Supply (Vin)

This signal is the input power supply to the QuickFire QF-200. It is at the same level as the power supplied to the board using the screw terminals (PL1) or the expansion bus if LK7 is fitted south. Care must be taken as this voltage can be up to 5 Volts.

6.3.10. Port A

This is put here just for completeness. All eight of the Port A channels are used in their special function mode as the lower 8-bits of the 68000 data bus. They are not available for use as general I/O channels, nor are they available on the Digital I/O connector.

6.3.11. Port B (PB2 – PB7)

Port B channels double up as some of the chip select signals, timer pins and PWM pins as shown in the table below. Port PB2 to PB7 can all be used as general purpose I/O channels if their special function is not required.

Channel	Special Function	General I/O
PB0	CSB0 – the on board RAM chip select	Not Available
PB1 / CSB1	CSB1 / SDWE Upper half of RAM chip select or Sequential DRAM Write Enable	Available
PB2	CSC0 / RAS0 Chip select group C lower	Available

	block chip select or RAS strobe for DRAM	
PB3	CSC1 / RAS1 Chip select group C upper block chip select or RAS strobe fro DRAM	Available
PB4	CSD0 / CAS0 Chip select group D lower block chip select or CAS strobe for DRAM	Available
PB5	CSD1 / CAS1 Chip select group D lower block chip select or CAS strobe for DRAM	Available
PB6	TIN / TOUT Timer input or output pin for both timer unit 1 and 2	Available
PB7	PWMO1 Pulse width modulation output for both PWM modules (see section 2.6 for details)	Available

6.3.12. Port C (PC0 – PC7)

The special functions for the Port C data lines tend to be related to the LCD module. All Port C signals are available for use as general-purpose I/O channels on the QuickFire QF-200.

Channel	Special Function	General I/O
PC0	LD0 LCD Data bus bit 0	Available
PC1	LD1 LCD Data bus bit 1	Available
PC2	LD2 LCD Data bus bit 2	Available
PC3	LD3 LCD Data bus bit 3	Available
PC4	LFLM LCD First line marker	Available
PC5	LLP LCD line pulse	Available
PC6	LCLK LCD shift clock	Available
PC7	LACD LCD Alternate crystal direction	Available

6.3.13. Port D (PD2, PD3, IRQ1)

The special function for the Port D signals are all to do with interrupts. All the channels in Port D have the capability to generate interrupts to the processor. Only four channel from Port D are available on this

connector, the other four are available on the expansion bus connectors. Channel PD0 doubles up as the Mode switch input (see section 6.3.7).

Channel	Special Function	General I/O
PD0 / MODE	INT0 Level 4 interrupt input	Available
PD1	INT1 Level 4 interrupt input	Available
PD2	INT2 Level 4 interrupt input	Available
PD3	INT3 Level 4 interrupt input	Available
PD4	IRQ1 Level 1 interrupt input	Available
PD5	IRQ2 Level 2 interrupt input	Available
PD6	IRQ3 Level 3 interrupt input	Available
PD7	IRQ6 Level 6 interrupt input	Available

6.3.14. Port E (PE0 – PE3)

The special function for port E channels is spit between SPI2 and UART1.

Channel	Special Function	General I/O
PE0	SPITXD SPI Transmitted data channel	Available
PE1	SPIRXD SPI Received data channel	Available
PE2	SPICLK2 SPI Clock signal	Available
PE3	DWE/UCLK DRAM Write Enable or UART Clock (synchronous use of UART)	Available
PE4 / RXD1	Serial Port received data input	Not Available
PE5 / TXD1	Serial Port transmitted data output	Not Available
PE6 / RTS1	Serial Port handshaking signal	Not Available
PE7 / CTS1	Serial Port handshaking signal	Not Available

6.3.15. Port F (PF0)

The special functions for the Port F channels vary between different modules in the processor. The table below shows the special function and which are available for use as general-purpose I/O channels on the QF-200.

Channel	Special Function	General I/O
PF0	LCONTRAST – An output generated by the LCD PWM to generate the contrast voltage	Available
PF1 / IRQ5	IRQ5 Level 5 Interrupt input	Available
PF2 / CLK	CLKO Clock Output from the processor for synchronising peripherals	Not Available
PF3 / A20	Upper 68K address line	Not Available
PF4 / A21	Upper 68K address line	Not Available
PF5 / A22	Upper 68K address line	Not Available
PF6 / A23	Upper 68K address line	Not Available
PF7 / CSA1	Chip select for the upper block of CSA. This can be used to select an expansion flash memory.	Not Available

6.3.16. Port G (PG2 – PG5)

The majority of Port G signals can be used for processor control and emulation. Most of these channels will affect the way that the processor starts up so care must be taken with the state of these signals at reset.

Channel	Special Function	General I/O
PG0 / DTACK	BUSW This channel determines the bus width of the boot address at reset. During normal operation it is used as the	Not Available

	DTACK signal	
PG1 / A0	This channel is used as the least significant address line for the 8-bit on board static RAM	Not Available
PG2	EMUIRQ. Emulator interrupt request (level 7). During reset if this signal is low the processor will start up in Emulator mode.	Available
PG3	HIZ/PD. A logic low during reset on this signal will put the processor into high impedance mode. During normal operation in emulator mode this channel indicates whether the current cycle is in program space or data space.	Available
PG4	EMUCS Used to select the dedicated memory space between $FFFC0000 and $FFFDFFFF	Available
PG5	EMUBRK Emulator break point. At reset if this signal is low the processor will start up in Bootstrap mode.	Available

6.3.17. Port J (PJ0 – PJ3)

The special functions for Port J signals are split between the SPI port 1 and the second UART serial port.

Channel	Special Function	General I/O
PJ0	MOSI SPI Master Out Slave In	Available
PJ1	MISO SPI Master In Slave Out	Available
PJ2	SPICLK1 bi-directional clock signal	Available
PJ3	SS Slave Select	Available
PJ4 / RXD2	Serial Port received data input	Not Available
PJ5 / TXD2	Serial Port transmitted data output	Not Available
PJ6 / RTS2	Serial Port handshaking signal	Not Available

PJ7 / CTS2	Serial Port handshaking signal	Not Available

6.3.18. Port K (PK0, PK4 – PK7)

Port K is another miscellaneous port that is used by a number of different modules.

Channel	Special Function	General I/O
PK0	DATA READY / PWMO2. Either the SPI data ready signal or the output from PWM unit 2	Available
PK1 / R/W	This signal is used as the R/W line from the controller.	Not Available
PK2 / DS0	This signal is used as the lower data strobe to validate the lower part of the data bus	Available
PK3 / DS1	This signal is used as the upper data strobe to validate the upper part of the data bus	Available
PK4	LD4 LCD data bus bit 4	Available
PK5	LD5 LCD data bus bit 5	Available
PK6	LD6 LCD data bus bit 6	Available
PK7	LD7 LCD data bus bit 7	Available

6.3.19. Port M (PM0 – PM5)

Port M signals double up as the external access to the memory controller.

Channel	Special Function	General I/O
PM0	SDCLK Sequential DRAM clock signal	Available
PM1	SDCE Sequential DRAM clock enable	Available
PM2	DQMH SDRAM input / output mask	Available
PM3	DQML SDRAM input / output mask	Available
PM4	SDA10 SDRAM Address A10	Available
PM5	DMOE DRAM continuous page mode output enable	Available

7. Indicator LEDs

The QuickFire QF-200 has five red LED indicators. These can be used to give an indication of the state of operation of the controller board. All LEDs are enabled or disabled using switch SW2A. Each LED has a 1KΩ current limiting resistor.

7.1. Power On Indicator (D1)

This LED is connected across the power supply. When the LEDs are enabled and the power is on this LED will be illuminated.

7.2. Operational Indicator (D3)

This red LED is connected to one of the processor general-purpose I/O channels (PD2 / INT2). When the LEDs are enabled, by toggling this I/O channel (while set to general I/O) under program control this LED can be toggled on and off to give an indication that an application is running.

7.3. RXD1 Indicator (D5)

This red LED is located next to the PL6 serial port connector. When there is any activity on the RXD line of serial port 1 this LED will flash if the LEDs are enabled.

7.4. TXD1 Indicator (D7)

This red LED is located next to the PL6 serial port connector. When there is any activity on the TXD line of serial port 1 this LED will flash if the LEDs are enabled.

7.5. RXD2 Indicator (D4)

This red LED is located next to the PL5 serial port connector. When there is any activity on the RXD line of serial port 2 (TERM) this LED will flash if the LEDs are enabled.

7.6. TXD2 Indicator (D6)

This red LED is located next to the PL5 serial port connector. When there is any activity on the TXD line of serial port 2 (TERM) this LED will flash if the LEDs are enabled.

8. Switches

There are a total of five switches on the QuickFire QF-200.

8.1. Reset Switch (SW1)

This switch will generate a manual reset to the controller. It is a push button switch. To reset the controller this switch must be pressed and held for 0.5 seconds. When the switch is released the processor will start operating again. Immediately following the reset all processor registers will be in their reset state, please refer to the 68VZ328 user manual for details of the reset state of each register following a reset. The operating system or start up code will then take over and set the processor registers up as required. Finally the application program will run and perform its own register modifications. During this start up time I/O channels may be driven differently to that required by the final application.

8.2. Option Switches (SW2)

There are four option switches on the QF-200 controller in a single bank of four switches. These switches will require a small tool to operate them so that they are not easily knocked.

8.2.1. LED Enable (A)

When this switch is in the ‘On’ position all the LEDs on the controller board are operational. When the switch is in the ‘Off’ position none of the LEDs will illuminate. For minimum current consumption this switch must be set in the ‘Off’ position. When the switch is in the ‘On’ position the current consumption will increase by a minimum of 1.8 mA (worst case 9 mA).

8.2.2. Mode Select (B)

When this switch is in the 'On' (Run) position the operating system will run a custom defined turnkey application from reset if one exists. When the switch is in the 'Off' (Debug) position a development environment ('shell') will run from reset. During code development, rather than keep moving this switch, LK1 forms a by pass link which can be fitted to put the board into 'Run' mode and removed to be back in 'Debug' mode. If the link option is used the switch must be set in the 'Off' position. This switch / jumper only has a special meaning just after a reset when the shell program reads the status of the channel. After this the application program can use the switch if required. The switch is connected to general-purpose I/O channel PD0 / INT0.

8.2.3. Bootstrap (C)

This switch is used to enable the bootstrap mode of operation. Bootstrap mode is an internal mode which bypasses the normal 68000 vector table from reset and enables commands to be downloaded directly to the processor using either of the on board serial ports. For more details on the bootstrap mode please refer to section 11. The operation of this switch only has special meaning when the processor is being reset. After this the application program can use the switch if required. The switch is connected to general-purpose I/O channel PG5.

8.2.4. Power Down Interrupt (D)

Switch four of the bank enables the power down interrupt. This can be used to generate an interrupt to the processor when the external power supply is failing. It can be used to put the processor and peripherals into a low power mode of operation if the controller is being run from an external battery source.

9. Links

There are eight links and jumper options on the QuickFire QF-200 controller.

9.1. Operation Mode (LK1)

This link forms a by pass to the Mode select switch (SW2 bank B). If the switch is set in the 'Off' position fitting a jumper on these two pins can be used to put the board into 'Run' mode. If the jumper is not fitted and the switch is in the 'Off' position the board will be in 'Debug' mode. If the switch is in the 'On' position this link has no effect on the processor operation. The mode of operation is determined just after reset only. After this the switch / jumper can be used as required by the application software.

9.2. Power Input (LK2)

This is a three-way jumper link. When the jumper is fitted in the South (2 – 3) position the input power supply is connected to the voltage regulator. In this mode the input power supply can be up to 5 volts. When this jumper is fitted in the North position, the input power supply is connected directly to the electronics and must be 3 volts. Failure to set this link correctly could result in the controller being damaged.

9.3. Regulator Enable (LK3)

This is a three-way jumper link. When the jumper is fitted in the South (2 – 3) position the on board voltage regulator is enabled. When the voltage regulator is enabled the input power supply to the controller can be up to 5 volts. When the link is fitted North, the input power supply must be 3 volts and the voltage regulator is disabled. LK2 should also be set in the same position as this jumper. Failure to set this link correctly could result in the controller being damaged.

9.4. RS232 / RS485 (LK4)

This three-way jumper link is used to determine which serial buffer serial port 2 receives its data from. If the jumper is fitted North the data is received from the RS232 buffer. When the jumper is fitted South the data is received from the RS485 buffer. Data is transmitted using both buffers.

9.5. RAM Power (LK5)

This three-way jumper link is used to power the static RAM on the controller card. If the jumper is fitted East, then the static RAM is powered with the battery backed supply. When the jumper is fitted West the power supply pin on the static RAM is connected to ground. This setting can be used to clear the contents of the RAM. The link should not be fitted in the West position while the controller is powered up.

9.6. RS485 Terminator (LK6)

When the controller is being used in RS485 mode a terminating resistor is required on both ends of the RS485 transmission line to prevent signal reflections. To place a 120Ω termination resistor across the transmission line fit a jumper across these two pins.

9.7. Expansion Power (LK7)

This is a three-way jumper link. When the jumper is fitted in the North (1 – 2) position the expansion (back plane) connector power supply is 3 volts. When the link is fitted in the South position the expansion connector is powered with the same supply as the controller. If the regulator is enabled this can be up to 5 volts. Failure to set this link correctly could result in the controller being damaged.

10. I/O Signal Usage

The MC68VZ328 has 76 I/O channels that can be configured either as special function I/O channels or general purpose I/O. While the QuickFire QF-200 board is designed to give the user maximum access to the processor some of the I/O channels are used on the board. This section lists all the channels that are used, what they are used for and if they are configured as special purpose or general I/O.

10.1. PD0 / INT0

This channel is used on the QF-200 board as the Mode switch input. It is a general purpose I/O channel. This special function is only used immediately following a reset or power up, after this the application can use this channel as a general purpose I/O.

10.2. PD1 / INT1

This channel is used to drive the operating LED D3. The application program can use it at all times.

10.3. PD5 / IRQ5

This channel is a back plane interrupt under normal operation. It has a special function following a reset or a power up. If PD5 / IRQ5 is low as well as PD6 / IRQ6 (section 10.4) being low during a reset then the on board flash memory is swapped to the block $1000000 to $1FFFFFF. To allow the controller to boot up correctly an expansion memory must fill the space $0000000 to $0FFFFFF. This is to allow a Flash Formatter card to be used to configure the on board flash memory. To disable this operation the application must ensure that this channel is high during the reset.

10.4. PD6 / IRQ6

This channel is used as a back plane interrupt under normal operation. It has a special function following a reset or a power up. If this channel is low at the end of the reset pulse the system enables an expansion memory card containing more flash memory. The address of the flash memory on the expansion card depends on the status of PD5 / IRQ5 (section 10.3). The operating system will automatically check the expansion memory for programs and data modules if the interrupt is low at reset.

10.5. PG5 / EMUBRK

This channel is connected to SW2 bank C. It is used at reset to enable the bootstrap mode of operation. For more details on the bootstrap

mode please refer to section 11. To allow the processor to power up normally this channel must be held high during the reset. During normal operation this channel can be used by the application as required.

10.6. RXD1

This channel is allocated to its special function. It is used as the receiver data input for serial port 1 (S1). It is not possible to use this channel for any other purpose.

10.7. TXD1

This channel is allocated to its special function. It is used as the transmitter data output for serial port 1 (S1). If the special function is not required this channel can be used as a general purpose I/O channel.

10.8. CTS1

This channel is allocated to its special function. It is used as the hardware handshaking input for serial port 1 (S1). It is not possible to use this channel for any other purpose.

10.9. RTS1

This channel is allocated to its special function. It is used as the hardware handshaking output for serial port 1 (S1). If the special function is not required this channel can be used as a general purpose I/O channel.

10.10. RXD2

This channel is allocated to its special function. It is used as the receiver data input for serial port 2 (TERM). It is not possible to use this channel for any other purpose.

10.11. TXD2

This channel is allocated to its special function. It is used as the transmitter data output for serial port 2 (TERM). Although if the special function is not required this channel could be used as a general purpose I/O we would not recommend it.

10.12. CTS2

This channel is allocated to its special function. It is used as the hardware handshaking input for serial port 2 (TERM) when this serial port is in RS232 mode. In RS485 networking mode this channel is not used. It is not possible to use this channel for any other purpose.

10.13. RTS2

This channel is allocated to its special function. It is used as the hardware handshaking output for serial port 2 (TERM) when this serial port is in RS232 mode. In RS485 networking mode this channel is used to operate the tri state control for the RS485 buffer. If the special function is not required this channel can be used as a general purpose I/O channel.

10.14. Pull-up Resistors

Most of the I/O channels have pull-up or pull-down resistors that can be enabled within the processor. The signals listed here have external pull-up resistors fitted on the board. The table lists the signals, pull up resistor value and resistor identifier.

Signal	Value	Identifier		Signal	Value	Identifier
OE	10 K•	R10		PG3	3K3	R16
UWE	10 K•	R12		IRQ1	10 K•	R20
LWE	10 K•	R9		PG2	10 K•	R18
D15	10 K•	R8		CLK	10 K•	R7
D0 – 14	10 K•	RP1		DTACK	10 K•	R29
PD0 INT0	10 K•	R15		DS1	10 K•	R14
R/W	10 K•	R24		DS0	10 K•	R17

PAS	10 K•	R33		IRQ6	10 K•	R19
MAS	10 K•	R31		IRQ5	10 K•	R30
RESET	10 K•	R1		INT3	10 K•	R22
PD1 / INT1	1 K• (D)	R23		INT2	10 K•	R21
RXD1	1 K• (D)	R28		TXD1	1 K• (D)	R26
RXD2	1 K• (D)	R34		TXD2	1 K• (D)	R35

(D) This signal is connected to a LED with a current limiting resistor.

10.15. Reset Modes

When the board powers up or is reset the state of the following signals determine what mode the processor starts up in. The user must ensure that during reset or power up these signals are in their inactive state unless it is intended to enter the special mode.

Signal	Function at reset	Default mode
IRQ6	Detects a FlashFormatter card is fitted. When detected also uses IRQ5 (see below)	High
IRQ5	If a FlashFormatter is connected, if this signal is high the QuickFire boots using the on board Flash memory. If the signal is low the QuickFire boots using the Flash memory on the FlashFormatter board.	High
PG5 / EMUBRK	Enables the MC68Z328 Bootstrap mode of operation.	High
PG3 / HIZ / PD	Logic low on this signal puts the MC68VZ328 in Hi-Z mode, where all pins are tri stated after the reset.	High or not connected
PG2 / EMUIRQ	Logic low on this signal puts the MC68VZ328 in emulation mode. This is not supported by CMS on the QuickFire boards, refer to the	High

	User Manual for details if required.	

11. Bootstrap Operation

The MC68VZ328 processor has three modes of operation. The QuickFire processors do not support the 'Emulator Mode' of operation. Most processing and operating is performed in 'Normal Mode'. The other mode of operation is the 'Bootstrap Mode'.

12. Connectors

12.1. Power Input Connector (PL1)

The power input connector is a two way screw terminal block. The ground reference voltage should be connected to the screw terminal marked '0' on the PCB silk screen. The positive supply voltage should be connected to the terminal marked '+' on the silk screen. Care must be taken when connecting the power supply as the board does not have any protection against incorrect polarity on the supply. The input voltage should be in the range 2.7 to 5 Volts. Voltages greater than 3.3 Volts will require the on board voltage regulator to be enabled. Please refer to section 5 for details.

12.2. Digital I/O Connector (PL2)

For full details of the signals available on this connector please refer to section 6.3. The connector is a 64 way DIN41612 ab type 90 degree plug.

B Side	Pin Number	A Side
GND	1	GND
PB3	2	PB2
PB5	3	PB4
PB7	4	PB6
MODE	5	PD1
PC1	6	PC0

PC3	7	PC2
PC5	8	PC4
PC7	9	PC6
MR	10	Vin
PD3	11	PD2
PE1	12	PE0
PE3	13	PE2
OE	14	PF0
UWE	15	LWE
PG3	16	PG2
PG5	17	PG4
PJ1	18	PJ0
PJ3	19	PJ2
CSB1	20	CSA1
IRQ1	21	PK0
PK5	22	PK4
PK7	23	PK6
PM1	24	PM0
PM3	25	PM2
PM5	26	PM4
MAS	27	PAS
RXD2	28	RXD1
TXD2	29	TXD1
CTS2	30	CTS1
RTS2	31	RTS1
3 Volts	32	3 Volts

12.3. Local Expansion Connector (PL3)

For full details of the signals available on this connector please refer to section 6.1. The connector is a 64 way DIN41612 ab type vertical plug.

B Side	Pin Number	A Side
D0	1	D8
D1	2	D9
D2	3	D10

D3	4	D11
D4	5	D12
D5	6	D13
D6	7	D14
D7	8	D15
GND	9	GND
CLK	10	SCL
GND	11	A17
DS1	12	RESET
DS0	13	A18
R/W	14	A19
A20	15	A0
DTACK	16	A21
GND	17	A22
PAS	18	NMI
AS	19	IRQ6
A23	20	IRQ5
N/C	21	IRQ3
A16	22	IRQ2
SDA	23	A15
A7	24	A14
A6	25	A13
A5	26	A12
A4	27	A11
A3	28	A10
A2	29	A9
A1	30	A8
-12V	31	+12V
VCC	32	VCC

12.4. Module Bus Expansion Connector (PL4)

For full details of the signals available on this connector please refer to section 6.2. The connector is a 64 way DIN41612 ab type vertical plug.

B Side	Pin Number	A Side

D0	1	D8
D1	2	D9
D2	3	D10
D3	4	D11
D4	5	D12
D5	6	D13
D6	7	D14
D7	8	D15
GND	9	GND
CLK	10	SCL
GND	11	A17
DS1	12	RESET
DS0	13	A18
R/W	14	A19
A20	15	A0
DTACK	16	A21
GND	17	A22
PAS	18	NMI
AS	19	IRQ6
A23	20	IRQ5
N/C	21	IRQ3
A16	22	IRQ2
SDA	23	A15
A7	24	A14
A6	25	A13
A5	26	A12
A4	27	A11
A3	28	A10
A2	29	A9
A1	30	A8
-12V	31	+12V
VCC	32	VCC

12.5. Serial Port 1 (PL5)

The serial port connector is a 10 way vertical polarised boxed plug. It is suitable for mating with insulation displacement sockets with bump

polarisation. The signals A & B are the positive and negative RS485 signals. The remaining signals are all at RS232 levels.

Signal	Pin	Pin	Signal
A	10	9	GND
B	8	7	N/C
RTS	6	5	RXD
CTS	4	3	TXD
3 Volts	2	1	N/C

12.6. Serial Port 2 (PL6)

The serial port connector is a 10 way vertical polarised boxed plug. It is suitable for mating with insulation displacement sockets with bump polarisation. The signals are all at RS232 levels.

Signal	Pin	Pin	Signal
N/C	10	9	GND
N/C	8	7	N/C
RTS	6	5	RXD
CTS	4	3	TXD
3 Volts	2	1	N/C

13. Specification

13.1. Processor

MC68VZ328 embedded controller
33 MHz clock speed
up to 5.4 MIPs

13.2. Memory

Flash Memory
1 M-byte on board programmable
512 k-byte x 16-bit configuration
2 Wait States
Expandable up to 2 M-bytes

Static RAM
512 k-bytes on board
512 k-bytes x 8-bit configuration
0 Wait States
Expandable up to 1 M-byte
Battery backed for minimum 28 days storage

13.3. Serial Ports

1 RS232 and 1 RS232/RS485 Serial Ports
Baud rates selectable between 600 and 115200 baud
Data format 7 or 8 bits / character
1 or 2 Stop bits
Odd, Even or No Parity
Automatic standby for buffers
RS232 Full duplex operation
RS232 Hardware handshaking
RS485 Half duplex operation
RS485 Automatic receiver enable / transmitter disable

13.4. Timers

Two user configurable timer / counters
16-bit Counters
30 ns resolution @ 33 MHz clock speed
Timer Input / Timer Output pin

13.5. General I/O

Up to 50 general purpose I/O channels
3 Volt operation

13.6. Liquid Crystal Display

Standard panel interface
Support for single monochrome LCD panels
Maximum panel size 640 x 512 pixels
Interface with 1, 2, 4 or 8-bit LCD data
16 simultaneous greyscale levels from a palette of 16 density levels
Hardware panning
8-bit PWM for contrast adjustment
Supports self refresh panels.

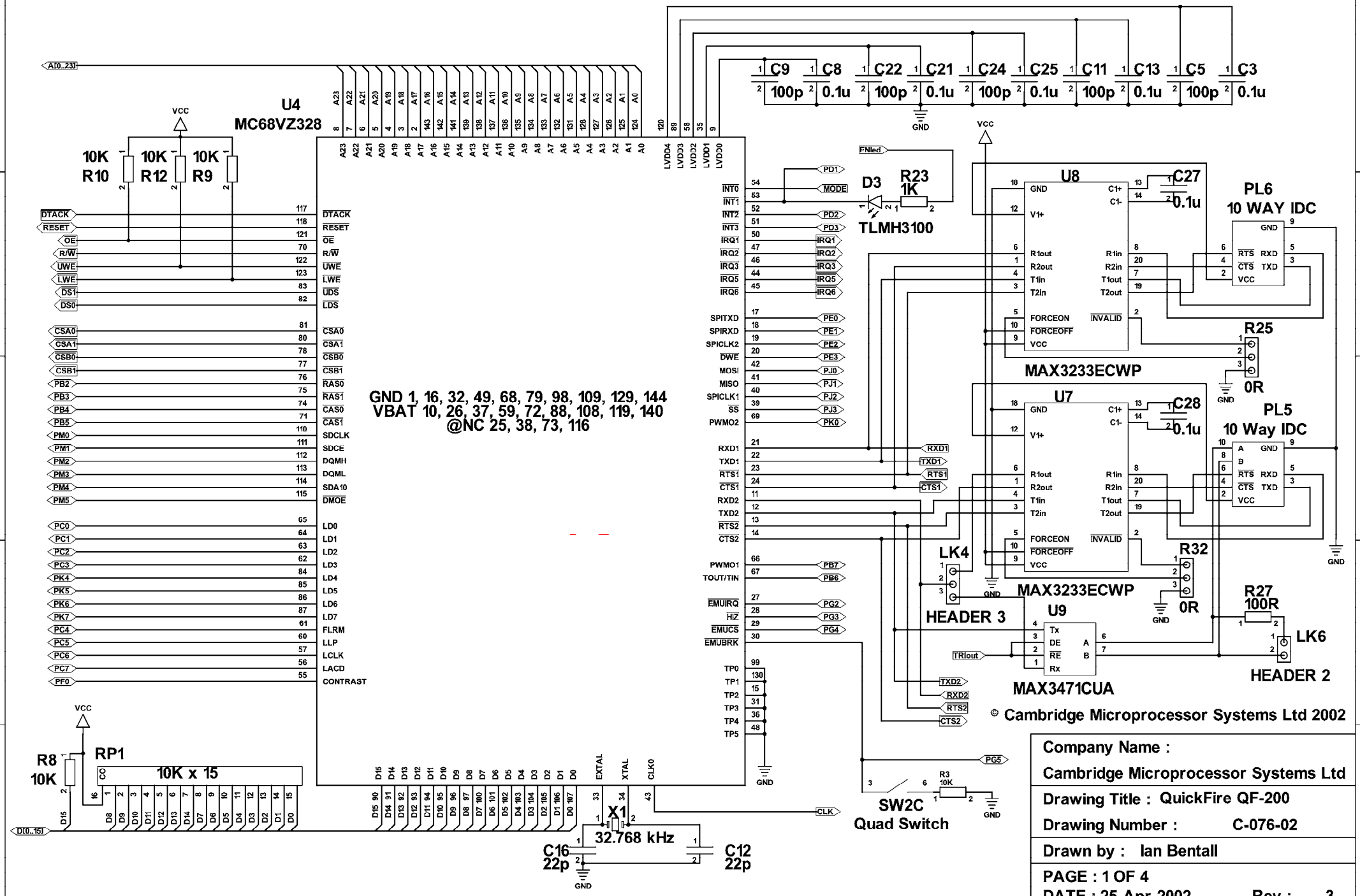
13.7. Battery

Vanadium Lithium Compound
Very low self discharge rate
20 mAh rated performance
Minimum 28 days data storage
Trickle charged while powered.

13.8. Environmental

3 Volt only operation	@ xxxmA
with LEDs enabled	@ xxxmA
Operating Temperature	0 to 70 °C
Relative Humidity	10 – 90% RH (non condensing)

14. Circuit Diagrams


U4
MC68VZ328
GND 1, 16, 32, 49, 68, 79, 98, 109, 129, 144
VBAT 10, 26, 37, 59, 72, 88, 108, 119, 140
@NC 25, 38, 73, 116
10K R10
10K R12
10K R9
D3
R23 1K
TLMH3100
U8
MAX3233ECWP
U7
MAX3233ECWP
U9
MAX3471CUA
C27 0.1u
C28 0.1u
PL6 10 WAY IDC
PL5 10 Way IDC
R25 0R
R32 0R
R27 100R
LK4
HEADER 3
LK6
HEADER 2
R8 10K
RP1 10K x 15
X1 32.768 kHz
C16 22p
C12 22p
SW2C Quad Switch
R3 10K
C9 100p
C8 0.1u
C22 100p
C21 0.1u
C24 100p
C25 0.1u
C11 100p
C13 0.1u
C5 100p
C3 0.1u
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Drawing Number : C-076-02
Drawn by : Ian Bentall
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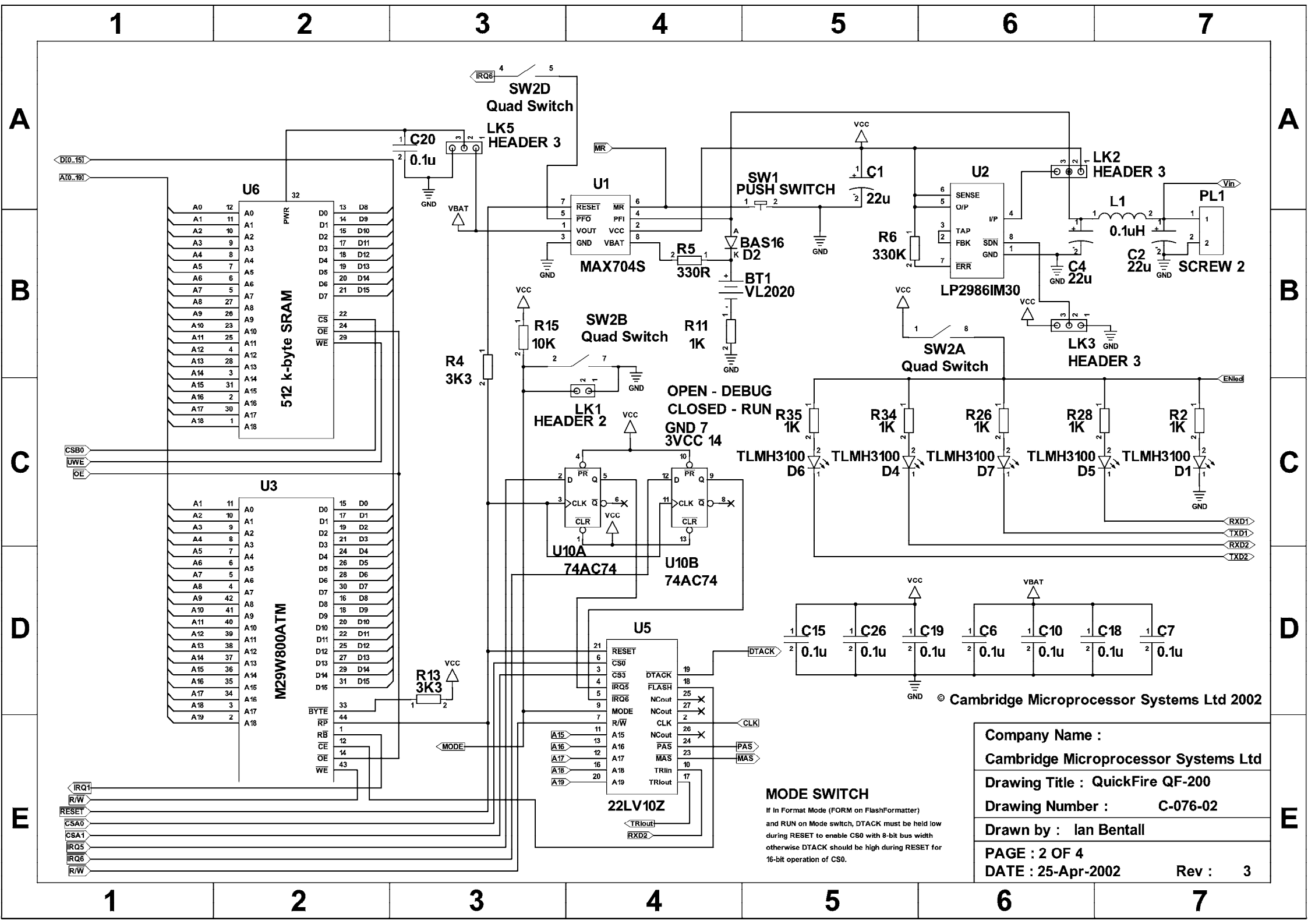
Rev : 3


SW2D
Quad Switch
LK5
HEADER 3
C20
0.1u
U6
512 k-byte SRAM
U3
M29W800ATM
U1
MAX704S
SW1
PUSH SWITCH
C1
22u
U2
LP2986IM30
LK2
HEADER 3
L1
0.1uH
PL1
SCREW 2
C2
22u
C4
22u
R6
330K
R5
330R
BAS16
D2
BT1
VL2020
R15
10K
SW2B
Quad Switch
R11
1K
R4
3K3
LK1
HEADER 2
OPEN - DEBUG
CLOSED - RUN
GND 7
3VCC 14
SW2A
Quad Switch
LK3
HEADER 3
R35
1K
R34
1K
R26
1K
R28
1K
R2
1K
TLMH3100
D6
TLMH3100
D4
TLMH3100
D7
TLMH3100
D5
TLMH3100
D1
U10A
74AC74
U10B
74AC74
U5
22LV10Z
R13
3K3
C15
0.1u
C26
0.1u
C19
0.1u
C6
0.1u
C10
0.1u
C18
0.1u
C7
0.1u
MODE SWITCH
If In Format Mode (FORM on FlashFormatter)
and RUN on Mode switch, DTACK must be held low
during RESET to enable CS0 with 8-bit bus width
otherwise DTACK should be high during RESET for
16-bit operation of CS0.
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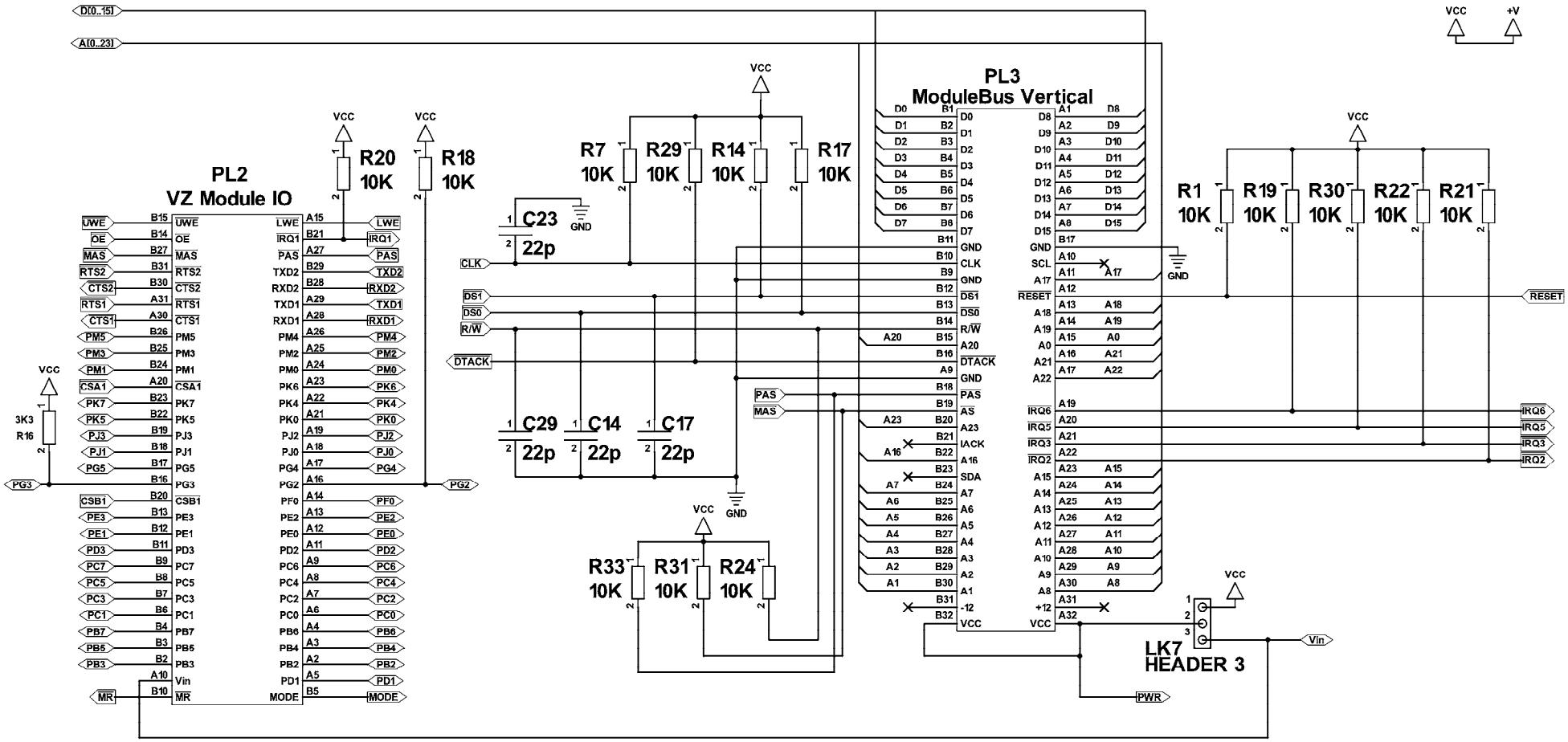

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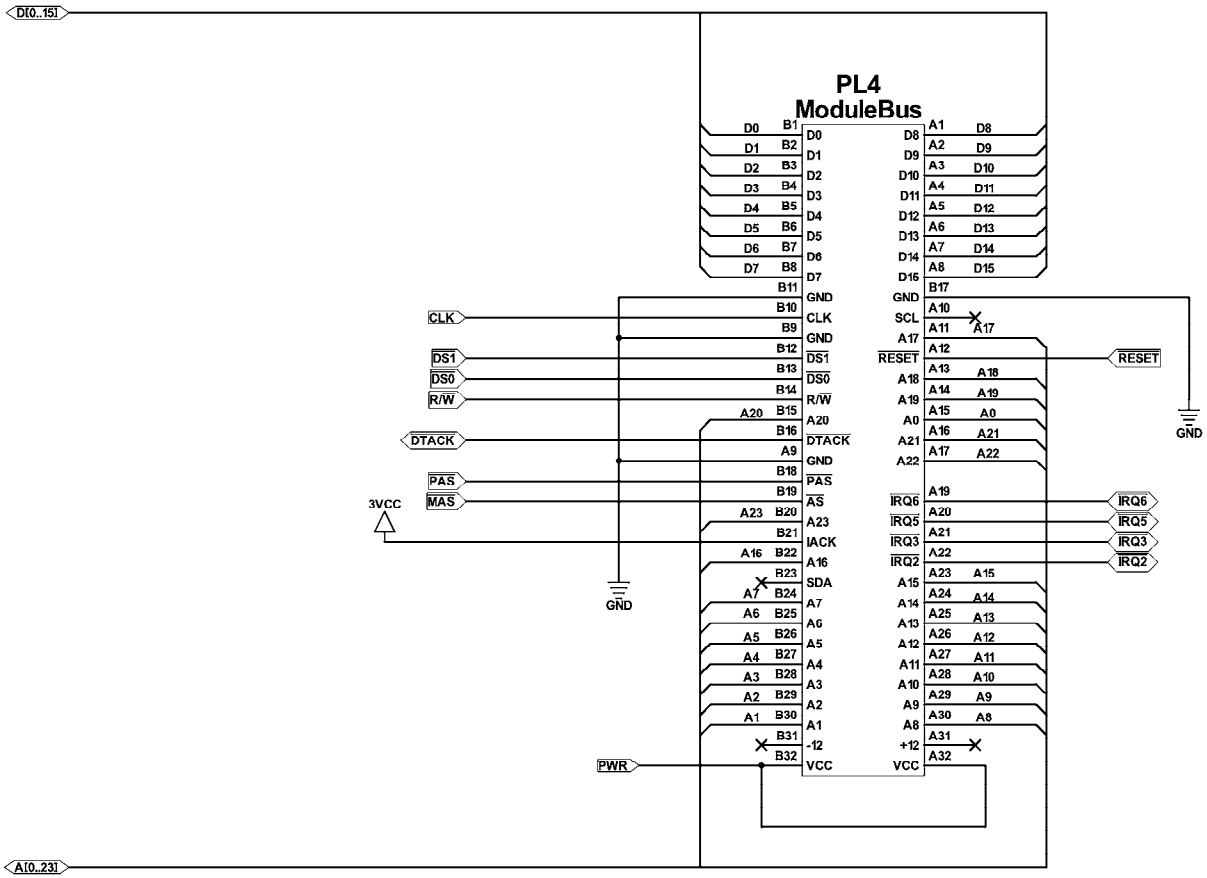

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