Measurement of Interrupt Response Time of PDP11/44 and PDP11/23 Computers with a CAMAC Interface

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Abstract:
Comparison of interrupt response times for PDP11/44 and PDP11/23+ machines, using the FORTH programming language, is presented. The interrupt response of the machines with FORTH implemented as a stand-alone operating system is compared with an implementation of FORTH running under the RSX11M operating system. The comparisons have been made on systems operating CAMAC parallel interface busses, both as single bus controllers (IEEE 583) and as parallel highways (IEEE 596), which require a branch driver interface.

The interrupt response of two DEC computers with FORTH implemented as a stand-alone operating system is compared with an implementation of FORTH running under the RSX11M operating system. The comparisons have been made on systems operating a CAMAC interface, both as a single-bus controller (IEEE 583) and as a parallel highway (IEEE 596). The measurements show that time overhead in response to interrupts is reduced by a factor of ~2 when stand-alone FORTH is used, compared to FORTH implementations under the RSX operating system.

There are two major configurations for CAMAC crate connections to a computer: the dedicated-interface configuration and the branch highway. The dedicated-interface configuration allows a computer to communicate with one crate controller, for control of the modules in a single crate, whereas the branch highway allows the computer to communicate with several crate controllers via a highway, which may be either a parallel or a serial bus link. Only parallel highway systems will be considered in this paper.

The configuration for testing the interrupt response is shown in Fig. 1. The tests were performed with a triggerable CAMAC analog-to-digital converter (Standard Engineering 212), which produces an interrupt after a conversion. The trigger for the ADC was produced by a TTL pulser, and the triggers were counted by a CAMAC scaler (Kinetic Systems 3640), which could be read from the computer. The trigger also started the sweep in an oscilloscope to provide a time reference. The action of the dataway could be monitored by a dataway display control (Kinetic Systems 3296), which gave a gate pulse when NAF codes selected by switches were detected on the dataway. The output of the dataway display control was counted in a second channel of the scaler and also displayed on the oscilloscope. Thus, time measurements could be made on the oscilloscope, and the scaler values

could be used to check that the number of triggers was the same as the number of dataway operations.

The timing-measurement results are shown in Table 1. All times are measured with respect to the ADC trigger pulse. The time to the first dataway cycle in the CAMAC crate represents the sum of the ADC conversion time, the interrupt latency of the processor, the software overhead in transferring control to the user's interrupt service routine, and the run time of the instructions required to set up and read the contents of the ADC output register. The ADC conversion time is 10 µs, and there is no appreciable delay in transferring a LAM seen by the crate controller to the computer bus interrupt lines.

The 'fast loop' times shown in Table 1 are the times between sequential ADC triggers when the 'fast loop' or overhead-free interrupt service cycles begin. This can be seen on the oscilloscope trace by increasing the trigger frequency until the exact time synchronism is lost between the first dataway cycle and the trigger pulse. This fast loop time represents the run time of the interrupt service process up to the test of the 'Lam sum' bit on the dedicated interface or the 'Bddyn' bit on the branch highway interface. Except for the register restore, interrupt enable (BIS), and return instructions, this is the whole run time of the ISR.

The third column of Table 1 shows the fastest interrupt frequency that can be obtained from the system and is measured as the time between triggers of the ADC at which interrupts begin to be missed or not serviced at all. This represents a condition when all interrupts are serviced in the 'fast loop' mode.

As can be seen from Table 1, there is a factor of about 2 increase in speed upon going from the 11/23 to the 11/44 regardless of which system is used, and stand-alone FORTH gives an increase of a factor of about 2 in speed over the RSX implementation on both the 11/23 and the 11/44. Since the interrupt service routines implemented for this test do few useful operations, they represent almost completely the overhead in processing interrupts from the CAMAC crates. The processor manual for the 11/23 indicates that the interrupt latency should be 9.75 µs. The ADC conversion time is 10 µs. The software overhead of the instructions in the ISR adds 9.75 µs overhead. This gives a hardware theoretical time to the first dataway operation of 46 µs, compared with the measured value of 50 µs. This shows that FORTH handles interrupts at the hardware speed of the machine, if implemented in the stand-alone configuration.

It is necessary to distinguish between interrupt response and maximum possible interrupt frequency. FORTH, as a stand-alone system, will always provide better interrupt response than the RSX implementation, but although the stand-alone system has roughly half the interrupt overhead

of the RSX implementation, if this overhead is a small fraction of the run time of the interupt service routine, the stand-alone system will not run at a much higher frequency than the RSX implementation. This is because the fastest interrupt service routines must be written in Assembler, and whether this is done from FORTH or by using a conventional assembler, the same machine code will result.

It is possible, with CAMAC, to run a PDP11/23 at an interrupt frequency of 14 kHz and a PDP11/44 at 30 kHz with the stand-alone FORTH and a minimal interrupt service routine. The corresponding figures for the RSX implementation of FORTH are 6.7 kHz for the 11/23 and 12.5 kHz for the 11/44.

Reference:

(1) J. R. Birkelund, J. A. Abate, and T. S. Lund, Proceedings of DECUS Symposium, Spring 1985, to be published.

FIGURE 1

TEST CIRCUIT

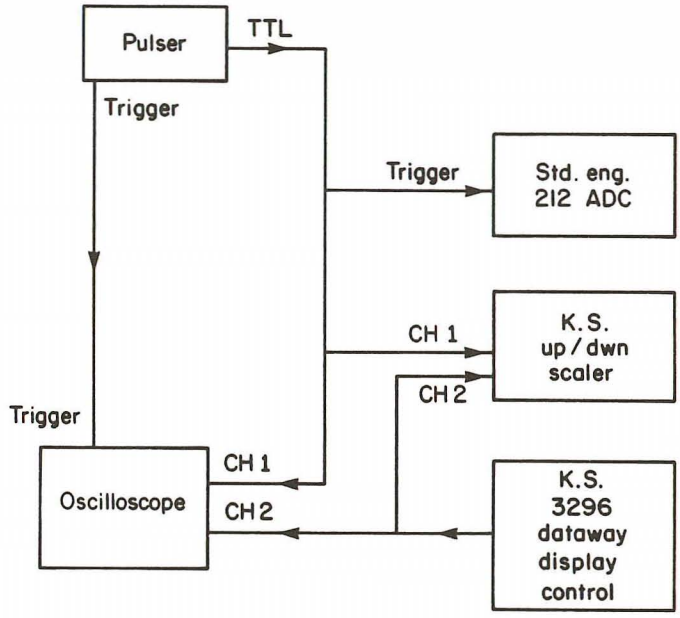

TABLE 1

PDPII INTERRUPT RESPONSE TIME (CAMAC)

TIMES IN μs AFTER ADC TRIGGER

DEDICATED INTERFACE (3920)

		1st Dataway Cycle	Fast Loop	Fastest
11/23	S.A.	50	90	70
11/23	RSX	100	170	150
11/44	S.A.	35.2	48.2	39
11/44	RSX	63.6	102.0	102

BRANCH HIGHWAY (411)

		1st Dataway Cycle	Fast Loop	Fastest
11/44	S.A.	25.2	45.0	33
11/44	RSX	53.8	103.2	80

These times include 10 μs for the ADC conversion time.