MVP MICROCODED CPU/16 ARCHITECTURE

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ABSTRACT

The MVP Microcoded CPU/16 is a 16-bit coprocessor board that directly executes high level stack-oriented programs. The CPU/16 may be micro-programmed to execute any stack-oriented language. FORTH was used as the initial implementation language to reduce development time and costs.

INTRODUCTION

Modern computer languages and compilers rely heavily on the concept of the push-down stack. However, conventional computers are optimized for register-oriented operations and impose large memory access time penalties when using stacks residing in main memory. The CPU/16 stack-oriented coprocessor can improve the performance of a personal computer to equal that of a much more expensive mini-computer for programs that make heavy use of stacks.

The MVP Microcoded CPU/16 was designed as a "low tech" exploration tool for stack-oriented processing. The result is an inexpensive commercial system that:

1) Uses simple, inexpensive, commonly available components.
2) Minimizes hardware and software development tool costs.
3) Fits the basic system onto a single IBM compatible Personal Computer expansion board (13" x 4").
4) Maximizes flexibility and minimizes complexity.
5) Achieves a 20 to 50 times speed improvement over 8088 MVP FORTH.

SYSTEM ARCHITECTURE

The CPU/16 is implemented in only 74 ICs (with 8k words of program memory), with no custom or semi-custom chips required. 74xx and 74LSxx series ICs provide all logic functions, with 120ns CMOS static RAMs for microcode and program memory.

Figure 1 shows the architectural structure of the CPU/16. All data paths are 16 bits wide.

The CPU/16 plugs into an IBM compatible personal computer as a one-slot expansion board. The host interface on the CPU/16 allows the personal computer to alter registers and memory as well as single-step programs at the microcode or macrocode level. When the CPU/16 is in

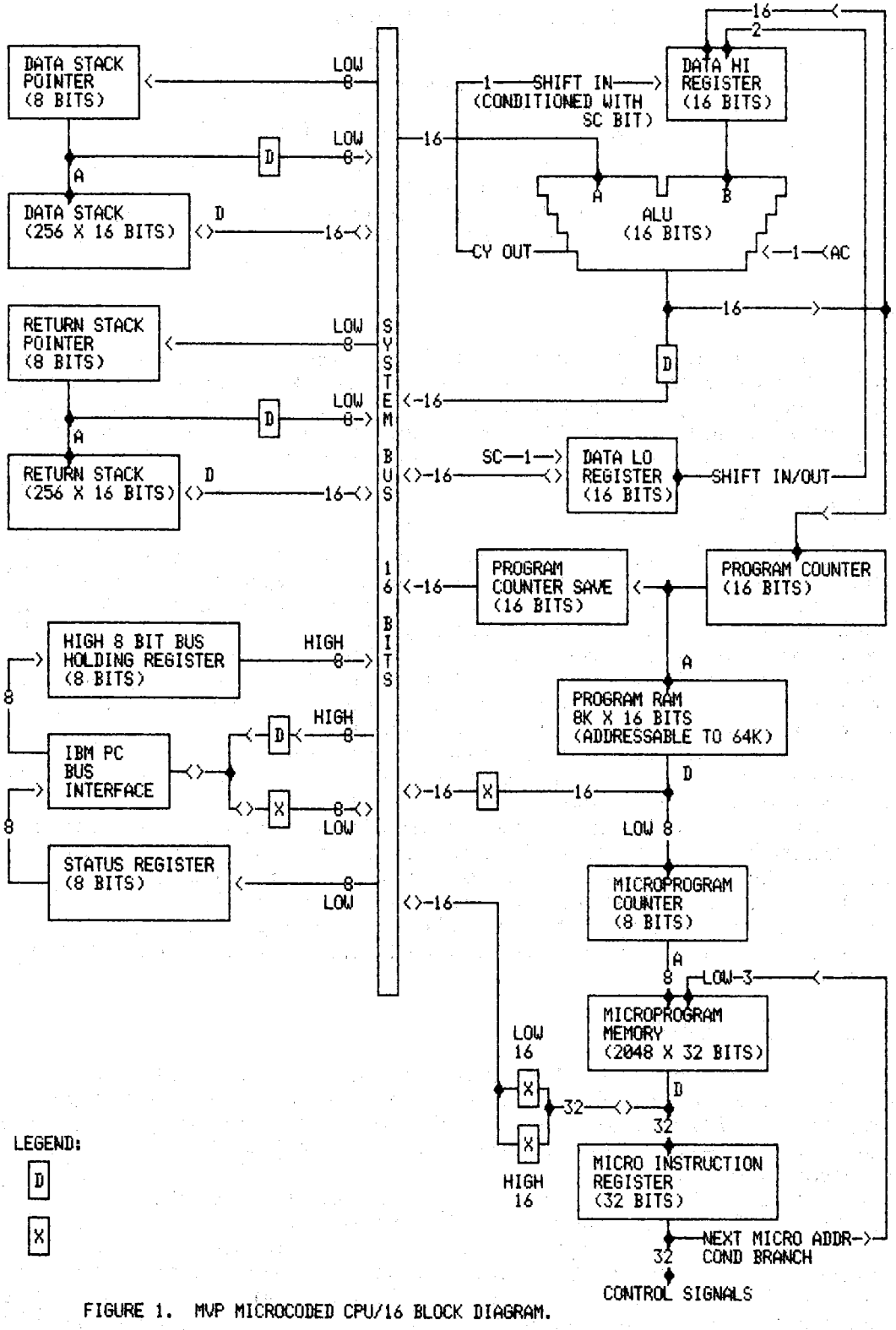

FIGURE 1. MVP MICROCODED CPU/16 BLOCK DIAGRAM.

"master" mode, the personal computer waits for the CPU/16 to request I/O service through the status register.

The return stack and data stack are hardware stacks with 8-bit pointers addressing 256 elements of stack memory. The stacks may be accessed and pointers incremented or decremented in a single clock cycle.

The ALU is built from 74LS181 chips, and has two shift registers to hold intermediate results. The Data Hi register and the Data Lo register can be shifted together as a 32-bit register for multiplication and division. The Data Hi register normally contains the top data stack element.

Program memory is organized as 64k words of 16 bits. All but the last 256 words may be used for program memory. A 16-bit program counter is used for all memory access addressing. The separate memory address bus from the program counter allows overlapped instruction fetching and execution. Program memory expansion beyond 8k words requires a daughter-board.

Micro-program memory is organized as 2k words of 32 bits. The microcode bit format is typical of modern horizontally microcoded machines. The micro-program counter and micro-instruction register allow overlapped fetching and execution of micro-instructions. Conditional microcode branches and microcode looping are accomplished by manipulation of the low order 3 bits of the micro-program address. If, during macro-instruction decoding, the highest 8 bits of a macro-instruction are not all 1, the microprogram counter is forced to all zero's, executing a DOCOL subroutine call. If the highest 8 bits are all 1, then one of 256 possible microcoded primitives is executed.

SOFTWARE SUPPORT

FORTH was picked as the CPU/16's development language for its efficiency, its simplicity of compiler implementation, and its friendly interactive environment with easy access to hardware resources. The CPU/16 supporting software includes a host control program, a microcode assembler, and a FORTH cross-assembler, as well as the FORTH microcode and kernel for the CPU/16 implementation.

The host program, microcode assembler, and cross-compiler are written in 8088 MVP-FORTH. The CPU/16 currently uses an MVP-FORTH kernel that differs in functionality from the 8088 MVP-FORTH version in that it uses word-oriented instead of byte-oriented memory addressing. In addition to FORTH, the CPU/16 is capable of supporting other programming languages such as Modula 2, Pascal, Lisp, and C. Any compiler implemented in machine-independent MVP-FORTH can be quickly installed on the CPU/16.

Current applications available on the CPU/16 include double-precision and quad-precision integer arithmetic and single-precision floating point math packages.

PERFORMANCE

The CPU/16 runs at a 4.77 MHz micro-cycle rate. An "average" microcoded primitive executes in 3 clock cycles (630 ns). This provides approximately a 20 to 50 times speed increase over 8088 MVP-FORTH programs operating at the same clock speed.

Since only half of the micro-program memory is required for the MVP-FORTH implementation, custom-written microcoded primitives may be added to a user's application to increase the speed of commonly used words. As an example, software stack manipulation words:

```
: INC[@]  ( PTR-ADDR -> N )   DUP  @ @  1  ROT +! ;
: DEC[!]  ( N PTR-ADDR -> )   -1  OVER +!  @  ! ;
```

can each be implemented in 10 micro-cycles (2.10 us), a speed increase of greater than 300% over high-level definitions. The listing for INC[@] is given as an example of CPU/16 microcode:

```
177 OPCODE: INC[@]     ( ADDR -> N )
0 :: SOURCE=ALU  ALU=B   DEST=PC  ;;    \ PC <- ADDR
1 :: SOURCE=ALU  ALU=-1  DEST=DLO ;;    \ DLO <- -1
2 :: SOURCE=RAM  ALU=A+1 DEST=DHI ;;    \ DHI <- POINTER+1
3 :: SOURCE=ALU  ALU=B   DEST=RAM ;;    \ POINTER <- DHI
4 :: SOURCE=DLO  ALU=A+B DEST=PC  INC[MPC]  ;;  \  PC <- PTR
5 ::  JMP=000  ;;     \ WAIT FOR RAM ACCESS, JMP TO NEXT PAGE
178 CURRENT-PAGE !
0 :: SOURCE=RAM           DEST=DLO ;;    \ DLO <- DATA
1 :: SOURCE=PCSAVE ALU=A+1 DEST=PC ;;  \ RESTORE PC
2 :: SOURCE=DLO ALU=A DEST=DHI DECODE ;;  \ T.O.S. <- DATA
3 ::    END ;;                \ JMP TO NEXT INSTRUCTION
```

FUTURE DEVELOPMENTS

Future developments for the CPU/16 will focus on broadening the range of languages and application programs available. Potential applications for a stack-oriented processor include: artificial intelligence, computer graphics, image processing, real-time control, and efficient execution of modern computer languages.

The CPU/16 is the first in a family of stack-oriented processors. A 32-bit general-purpose stack-oriented processor with greater speed and memory addressability is currently in development.

CONCLUSIONS

The MVP Microcoded CPU/16 is a high performance, general-purpose stack-oriented processor. A "low tech" approach has yielded significant speed improvements over current microprocessors at a modest cost. Compatibility with existing MVP-FORTH systems allows for easy porting of existing software to a high performance environment.