Letters

To the editor:

This letter is in response to the excellent article "User-Oriented Suggestions for Floating-Point and Complex-Arithmetic Forth Standard Extensions", which appeared in Vol. 3, No. 4 of *Journal of Forth Application and Research*.

In this article the authors state that overflow of the Intel 8087 numeric coprocessor 8-deep F-stack "is not signalled in any useful manner" (p. 67) and that "the 8087 was not designed to deal with this problem" (p. 76). In both of these statements, the authors are in error.

For the case of the 8087, the INT pin (pin 32) can signal an exception condition when *any* 8087 invalid operation occurs. This signal will occur if the proper bit in the interrupt-enable mask in the 8087 control word is set equal to zero. In the case of an IBM PC or XT, an active 8087 INT signal is passed to the NMI pin of the 8088 central processor. This in turn will cause the 8088 to transfer control to the address pointed to by the NMI interrupt vector (interrupt number 2).

The 80287 handles exceptions by directly transferring to the address pointed to by the interrupt number 16 vector. In the case of an IBM AT, a routine in ROM transfers control to the address pointed to by the NMI interrupt vector. This allows interrupt handler code to be the same for both the IBM PC and AT.

Note that by using an interrupt handler, there is *no* execution time overhead in floating point exception monitoring. I am sure that several (or most) Forth vendors have implemented this method of exception checking, and definitions such as `?OVERFLOW` should not be necessary.

Sincerely,

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