

The Implementation of a Parallel Architecture for the OPS Expert System Language*

John D. Allen and Philip L. Butler

A parallel processor was designed and built at Oak Ridge National Laboratory for high-speed execution of the OPS expert system language. The parallel architecture is presented along with the first implementation of this architecture.

The first implementation is based on the Motorola MC68000 microprocessor. A custom board was designed that contains four MC68000's each with 512K bytes of memory. There are currently 16 boards in the system for a total of 64 processors. These parallel "rule processors" are controlled by a single Host system, which is a conventional Multibus 68000 computer. This control is through a single Interface Board which allows minimal replication of control and addressing logic.

The OPS language has been implemented in Forth to run on the parallel processor system. The Host system parses the OPS rules and places the left-hand sides of each rule into a rule processor. The rule right-hand sides remain in the Host system for eventual firing. The OPS recognize-act cycle then becomes a cycle between the single Host system and a number of parallel rule processors.

* Research sponsored by the U.S. Department of Energy, under contract DE-AC05-84OR21400 with Martin Marietta Energy Systems, Incorporated.